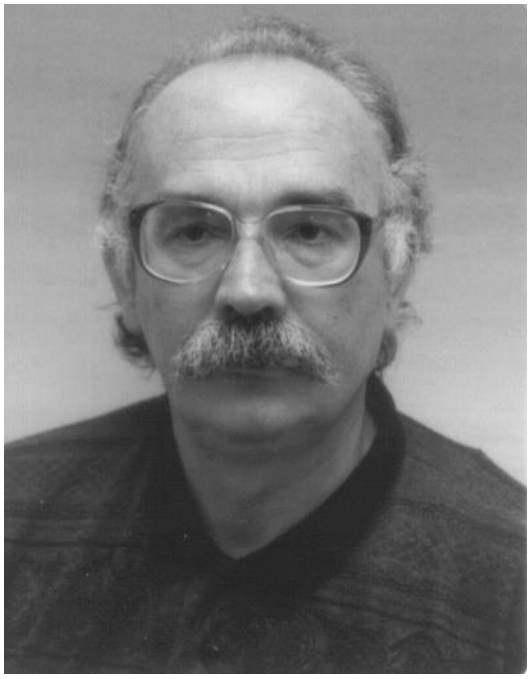
Vančo B. Litovski

Professional biography

1970.-2014.

Contents



Prof. Vančo B. Litovski

http://leda.elfak.ni.ac.rs

1. Short biography

Prof. Litovski was born in 1947in Rakita, South Macedonia, Greece. Primary scool and „gymnasium“ he graduated in Bitola, Republic of Macedonia. He enrolled the Faculty of Electronic Engineering in Niš in 1965 where he graduated in March 1970. He was appointed teaching assistant at the Chair of Electronics at the Faculty of Electronic Engineering in Niš on March 20, 1970. He got his Magisterium in June 1974. He served his one year obligatory military service in 1974/75. He got his Ph.D. in June 1977; He was elected a full professor at the Faculty of Electronic Engineering in Niš in 1987 he was appointed visiting processor at the University of Southampton, UK, on November 1999. He was performing the duty of head of the Chair of Electronics at The Faculty of Electronic Engineering in a period of 12 years. He wa steaching the following subjects “Electronics I“ , “Design of electronic circuits“, “Physical bases of electronics”, “Amplifiers”, “Testing of Electronic circuits”, “Neural networks” and “System on chip design”. He was teaching also at the Universities of Priština, Sarajevo, Novi Sad, and Banja Luka.

As an expert he was serving for several years as a consultant for research and development of the CEO of “Elektronska Industrija Niš“.

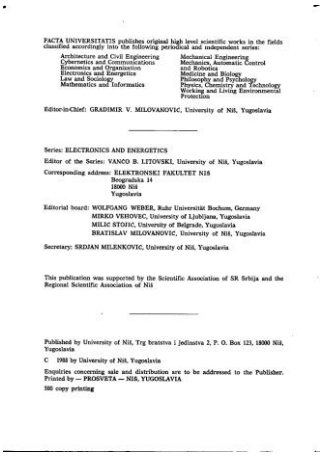
Prof. Litovski was member “The Institute of Electrical and Electronic Engi-

neers “ for 20 years, and member of “The Association for Computing". He is member of the presidency of ETRAN. He was the founder and the first president of the Yugoslav Simulation Society.

Prof. Litovski is regular member of the Academy of Engineering Sciences of Serbia.

He is winner of several awards delivered by the Town of Niš, The University of Niš, and The Faculty of Electronic Engineering (in 1966, 1967, 1980, 1985, and 1995. he got similar recognitions from the faculties of Electrical Engineering of Banja Luka and Eastern Sarajevo for special contribution to the development of these faculties. He got a special recognition of the journal “TEHNIKA” in 1985 and the ETRAN award in 1986. He got the “High recognition” from ETRAN for special contribution to the cause of ETRAN. He was awarded the “Tesla” award given by the independent Tesla foundation, for “exceptional achievements in engineering and technology” in 1994. On July 1998 he was awarded the “Savastano” award for best paper published in the previous three years period, by The European Federation of Simulation Societies.

His efforts in improving the quality of teaching wherever he was engaged were mostly expressed by implementation of investments via European projects. He was in charge for the University of Niš’s part of the projects TEMPUS_JEP-17028-2002 and TEMPUS_JEP_41107-2006. He was also i charge for the project CDP+ N° 20/IS/06, financed by WUS Austria for the Faculty of Electrical Engineering in Eastern Sarajevo.


FACTA UNIVERSITATIS publishes original high level scientific works in the fields classified accordingly into the following periodical and independent series:

Architecture and Civil Engineering
Cybernetics and Communication
Economics and Organization
Electronics and Energetics
Law and Sociology
Mathematics and Informatics
Mechanical Engineering
Mechanics, Automatic Control and Robotics
Medicine and Biology
Philosophy and Psychology
Physics, Chemistry and Technology
Working and Living Environmental Protection

Editor-in-Chief: GRADIMIR V. MILOVANOVIC, University of Niš, Yugoslavia

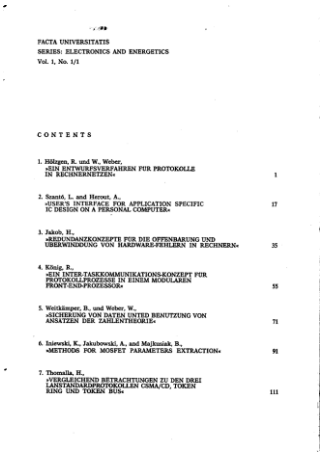
Series: ELECTRONICS AND ENERGETICS
Editor of the Series: VANCO B. LITOVSKI, University of Niš, Yugoslavia
Corresponding address: ELEKTRONSKI FAKULTET NIŠ
Beogradska 14
18000 Niš
Yugoslavia

Editorial board: WOLFGANG WEBER, Ruhr Universität Bochum, Germany
MIRKO VEHOVEC, University of Ljubljana, Yugoslavia
MILIC STOJIC, University of Belgrade, Yugoslavia
BRATISLAV MILOVANOVIC, University of Niš, Yugoslavia

Secretary: SRDJAN MILENKOVIC, University of Niš, Yugoslavia

This publication was supported by the Scientific Association of SR Srbija and the Regional Scientific Association of Niš

Published by University of Niš, Trg bratstva i jedinstva 2, P. O. Box 123, 18000 Niš, Yugoslavia
© 1988 by University of Niš, Yugoslavia
Enquiries concerning sale and distribution are to be addressed to the Publisher.
Printed by — PROSVETA — NIŠ, YUGOSLAVIA
500 copy printing


FACTA UNIVERSITATIS
SERIES: ELECTRONICS AND ENERGETICS
Vol. 1, No. 1/1

CONTENTS

Prof. Litovski founded and developed the first intenational journal in the field of electronics at the University of Niš: “Facta Universitatis, series: "Electronics and Energetics”. In addition he was a amember of the first editorial board of the journal “Elektronika“ which was published in a period of five years by Elektronska Industrija from Niš. He is also a member of the

editorial board of the journal „Electronics“ published by the Faculty of Electrical Engineering in Banja Luka.

Prof. Litovski proudly claims that he was the one who brought to the Faculty of Electronic Engineering: the computer graphics, the Unix operating system, the simulation of electronic circuits and systems, the design of electronic integrated circuits, The TCP-IP protocol, the supercomputing in Beowulf technology, the neural networks, and he was the first to introduce NIDAQ-LabView technology in laboratory teaching at the Faculty.

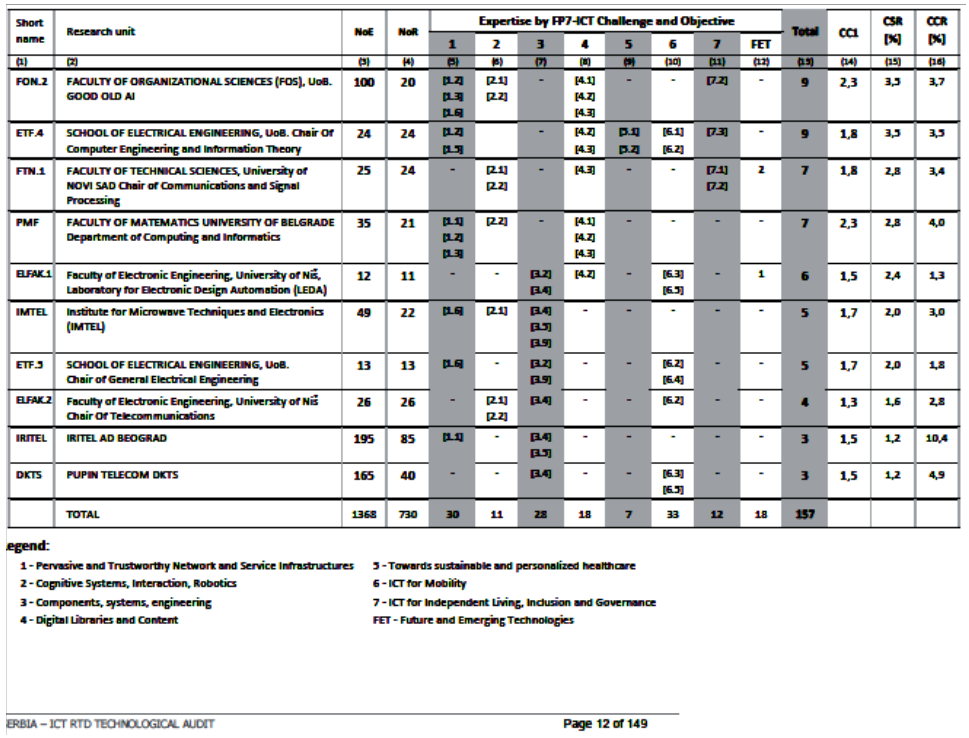
He was the first to establish a reasearch laboratory, LEDA, at the Faculty. In: Stephan Pacall (Advisor, Directoate C, »Lisbon strategy and policies for information society«), »Serbia – ICT RTD technological audit«, published by the European Comission Information Society and Media, on March 2010, LEDA was identified as one among 17 centers of exellence of Research and development in Serbia.
http://ebookbrowse.com/serbia-ict-rtd-technological-audit-final-report-pdf-d115707490

2. Scientific activities

The scientific opus of Prof. Litovskog is mainly related to design of electronic circuits and systems (discrete and integrated). Being a pioneer in the field he practically paved the research road for research in the subject in Serbia. In his earliest research phase he was investigating computer-aided synthesis of electronic communication filters. He made his doctoral thesis in that field while hes results were published in the most distinghuished journals in the USA and Yugoslavia. Together with his mentor Prof. Branko Raković he introduced a new class of filtering functions named Lest-Squares Monotonic (LSM). Toward the end of the seventies of the twentieth century, he started his research in integrated circuits design. The research work was performed within the Laboratory for electronic design automation (LEDA). In the field of CAD of electronic circuit thanks to his personal efforts and to efforts coordinated by him, the first Yugoslav electronic-circuit simulators were developed (named LIFT and MOST) in the early eighties. Ater that this research task was further fostered so that LEDA became a leading research center in the field. Software packages for simulation mixed-signal and mixed-level described circuit and systems developed in LEDA were implemented at several universities in Western Europe.

Automation of IC layout design was the next activity undertaken within LEDA. The first Yugoslav integrated software package for gate-array design named ISPGM was developed and implemented. It was presented as an invited lecture at the »3rd MidEuropean Custom Circuit Conference, in Sopron, 1991”. This package was directly used in the Nis Elektronska Industrija for

design CMOS gate arrays. Based on these results decisions were made at the federal level for investments into CAD equipment for electronic design.



Short name	Research unit	NoE	NoR	Expertise by FP7-ICT Challenge and Objective								Total	CCI	CSR [%]	CCR [%]
				1	2	3	4	5	6	7	FET				
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)
FON.2	FACULTY OF ORGANIZATIONAL SCIENCES (FOS), UoB. GOOD OLD AI	100	20	[1.2] [1.3] [1.6]	[2.1] [2.2]	-	[4.1] [4.2] [4.3]	-	-	[7.2]	-	9	2,3	3,5	3,7
ETF.4	SCHOOL OF ELECTRICAL ENGINEERING, UoB. Chair Of Computer Engineering and Information Theory	24	24	[1.2] [1.5]		-	[4.2] [4.3]	[5.1] [5.2]	[6.1] [6.2]	[7.3]	-	9	1,8	3,5	3,5
FTN.1	FACULTY OF TECHNICAL SCIENCES, University of NOVI SAD Chair of Communications and Signal Processing	25	24	-	[2.1] [2.2]	-	[4.3]	-	-	[7.1] [7.2]	2	7	1,8	2,8	3,4
PMF	FACULTY OF MATEMATICS UNIVERSITY OF BELGRADE Department of Computing and Informatics	35	21	[1.1] [1.2] [1.3]	[2.2]	-	[4.1] [4.2] [4.3]	-	-	-	-	7	2,3	2,8	4,0
ELFAK.1	Faculty of Electronic Engineering, University of Niš, Laboratory for Electronic Design Automation (LEDA)	12	11	-	-	[3.2] [3.4]	[4.2]	-	[6.3] [6.5]	-	1	6	1,5	2,4	1,3
IMTEL	Institute for Microwave Techniques and Electronics (IMTEL)	49	22	[1.6]	[2.1]	[3.4] [3.5] [3.9]	-	-	-	-	-	5	1,7	2,0	3,0
ETF.3	SCHOOL OF ELECTRICAL ENGINEERING, UoB. Chair of General Electrical Engineering	13	13	[1.6]	-	[3.2] [3.9]	-	-	[6.2] [6.4]	-	-	5	1,7	2,0	1,8
ELFAK.2	Faculty of Electronic Engineering, University of Niš Chair Of Telecommunications	26	26	-	[2.1] [2.2]	[3.4]	-	-	[6.2]	-	-	4	1,3	1,6	2,8
IRITEL	IRITEL AD BEOGRAD	195	85	[1.1]	-	[3.4] [3.5]	-	-	-	-	-	3	1,5	1,2	10,4
DKTS	PUPIN TELECOM DKTS	165	40	-	-	[3.4]	-	-	[6.3] [6.5]	-	-	3	1,5	1,2	4,9
	TOTAL	1368	730	30	11	28	18	7	33	12	18	157			

egend:

1 - Pervasive and Trustworthy Network and Service Infrastructures
2 - Cognitive Systems, Interaction, Robotics
3 - Components, systems, engineering
4 - Digital Libraries and Content
5 - Towards sustainable and personalized healthcare
6 - ICT for Mobility
7 - ICT for Independent Living, Inclusion and Governance
FET - Future and Emerging Technologies

ERBIA – ICT RTD TECHNOLOGICAL AUDIT Page 12 of 149

Prof. Litovski started research in electronic testing and design for testability in Serbia. The later is especially rlated to the introduction of the IEEE 1149.1 standard. His main research results in this area are related to establishment of methodology for fault modelling, fault simulation and its implementation within the system for automatic test pattern generation for analog and digital circuits. Recently he introduced electronic circuit diagnostic as a research subject in Serbia. He published the first textbook on the subject of testing and diagnosis of electronic circuits in serbian.

Implementation of artificial neural network in computer-aided design of electronic circuits and systems was a research subject where LEDA and Prof. Litovski gave a significant scientific contribution to the overall research efforts. The first international meeting on ANNs took place at the Faculty of Electronic Engineering in the year 1990. Prof. Litovski was the first to implement ANNs for electronic device modelling. In that way he opened a completely new way of black-box modelling of electronic components and circuits. The importane of these reults was broadly recognized. That may be confirmed by the fact that the British EPSRC granted a research project on this subject to Prof. Litovski in

the war year of 1999/2000.

Prof. Litovski was the first in Serbia to introduce research in the field of sustainable electronic design. His social engagement in the subject helped seriously to the recognition of the problem of the electronic waist and the need for sustainable and eco-electronic design in the Serbian community.

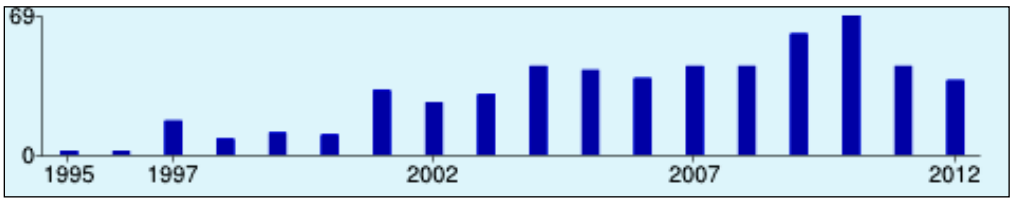
To his name is connected the implementation of ANNs for prediction based on short time series. These concepts were implemented for prediction in various fields such as electricity loads prediction, prouction of electrical energy, production of microelectronic components, prediction of technological developments in electronics, prediction in eco-developments etc.

Prof. Litovski published sveral hudreds of publications as can be seen from the lists below. He had 90 coauthors while the average number of authors per publication on his publications was around 2.7.

3. Citations

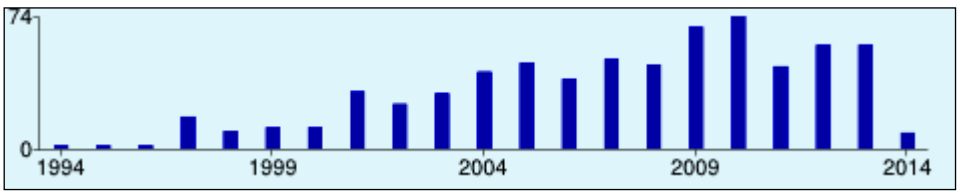
Here is a histogram created by Scholar Google containing all citations available to them with no selections. It is accurate but not precise and it covers a short period only.

http://scholar.google.com/citations?user=Z5IhjdYAAAAJ&hl=sr



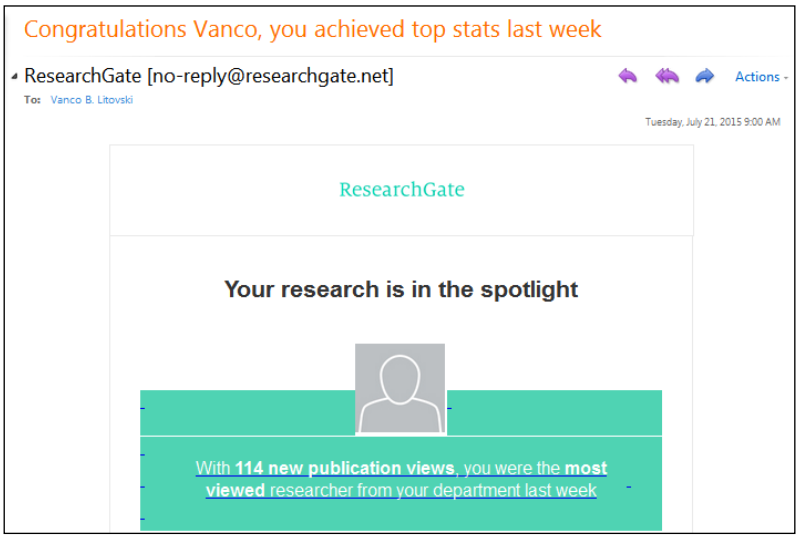
Citation indeces on March 21, 2014

	All	Since 2009
Citations	716	313
h-index	12	8
i10-inedex	19	5



Research gate has its own measure of V. Litovski's citation. On the same

date as bove it was: Your RG Score: 18.66. On July 21, 2015 (almost three years after retirement) Researchgate published the message bellow:



Next, a list of citations will be given with comments when appropriate. *In that list no self citations and citations by Prof. Litovski's coauthors are mentionned.*

i	**1**	The monograph: (**5.a.2**) "*VLSI Design*", Nauka, Beograd, 1991. (in Serbian), was cited: 1. In the paper: Melikian, V., "Logic *Simulation of Digital Circuits Exposed to Radiation*", Facta Universitatis, Series: Electronics and Energetics, Vol. 12, No.1, 1999, pp. 71-86, UDC 621.3.049.7
ii	**2**	The chapter in a monograph: (**5.a.5**) Andrejević Stošović, M., Litovski, V., ***"Electronic Circuits Diagnosis Using Artificial Neural Networks"*,** Micro Electronic and Mechanical Systems, Edited by Kenichi Takahata, Intech, ISBN 978-953-307-027-8, 2009, pp. 385-404, was cited in 1. Kovalyov, A., "*Training a neural network, oriented to solution of the problem of parameter identification of elements of analog devices*", Faculty of computer science and technology (CST), Department of computer engineering (CE), Donetski Nacionalen tehničeski Universitet, http://masters.donntu.edu.ua/2012/fknt/kovalyov_a/indexe.htm 2. Binu D., and Kariyappa, B. S. "A survey on fault diagnosis of analog circuits: Taxonomy and state of the art", AEU- Int. J. of Electronics and Communications, Vol. 73, March 2017, pp. 68-

		83.
iii	**1**	The paper: (**5.b.1**) Damnjanović, M.S., and Litovski, V.B., "*A survey of routing algorithms in custom IC design*", Journal of Semicustom ICs, Vol. 7, No. 2, 1989was cited: 1. In the report: S.P. Khatri, R. K. Brayton, A. Mehrotra, A. L. Sangiovanni-Vincentelli, and M.R. Prasad, "*Routing Techniques for Deep Sub-micron Technologies*", EECS Department **University of California, Berkeley** Technical Report No. UCB/ERL M99/15 1999 (http://www.eecs.berkeley.edu/Pubs/TechRpts/1999/3602.html) , it is written: "**Area routing techniques have been reviewed as part of several surveys on physical design [KO90, Oht86, DL89]".** With [DL89] the above was cited.
iv	**11**	The paper: (**5.c.1**) Raković, B.D., and Litovski, V.B., "*Least-squares monotonic low-pass filters with sharp cutoff*", Electronic Letters, Vol. 9, No. 4, pp.75-76, 1973, was cited: 1. In the paper: Козлов, М.В., „*Синтез Фільтрів, Які Використовуються При Спектральному Аналізі Шумів І Вібрацій*", Вісник ЖДТУ, Vol. 54, No. 3, 2010, ISSN 1728-4260, *Технічні науки*, стр. 50-59. 2. In the paper: Beccari, C., "*The use of the shifted jacobi polynomials in the synthesis of lowpass filters*.", Int. J. Circ. Theor., Appl., 7, 1979, pp. 289–295. 3. In the paper: Jovanović, V., Rabrenović, D., "*Lowpass-filter flat magnitude characteristic with sharp cutoff*", Electronics Letters, Volume 11, Issue 8, 17 April 1975, page 174, Print ISSN 0013-5194, Online ISSN 1350-911X. 4. In the paper: Djurich, B.M., "*Monotonic lowpass filters with maximum selectivity*", Electronics Letters, Volume 11, Issue 4, 20 February 1975, p. 82 – 83, DOI: 10.1049/el:19750062, Print ISSN 0013-5194, Online ISSN 1350-911X. 5. In the paper: M. Tomlinson "*The specification and design of filters for amplitude and phase modulated data transmission systems*,", Radio and Electronic Engineer, Volume 46, Issue 4, April 1976, p. 161 – 169, DOI: 10.1049/ree.1976.0027, Print ISSN 0033-7722. 6. In the paper: Nossek, J.A., Smolka, G.J. "*Q-enhancement and extension of the stability range of generalized immittance converters*", IEEE Trans. on Circuits and Systems, Vol. 27, Issue: 12 Dec 1980, pp. 1272 - 1274, ISSN : 0098-4094, DOI: 10.1109/TCS.1980.1084756.

		7. In the paper: Calisto Schwedersky e Sidnei Noceti Filho, "*Uma Nova Função de Aproximação Least Square com Zeros Imaginários Obtidos por Otimização*", XXVII Simpósio Brasileiro De Telecomunicações – SBrT 2009, 29.09. to 2.10. 2009, Blumenau, SC, http://www.eletrica.ufpr.br/anais/sbrt/SBrT27/-Sess%C3%B5es%20T%C3%A9cnicas_Artigos/Sess%C3%A3o%20T%C3%A9cnica_34/5_57733.pdf. 8. In the paper: Rabrenović, D. M., Aleksić, Ž. J., "*A method of improving transient characteristics of functions with monotonic magnitudes*", Int. J. of Electronics , Vol. 51, Iss. 1, 1981, pp. 1-13. 9. In the paper: Malvar, H., Caloba, L.P. "*Least-squares low-pass filters with nonmonotonic response*", IEEE Trans. on Circuits and Systems, Vol. 27, Dec. 1980, pp. 1270 - 1272, ISSN: 0098-4094. 10. In the paper: Kidambi, S.S., "*Simple method for design of monotonic analogue filters*", Electronics Letters, Vol. 36 , No. 4, 17 Feb. 2000, pp. 287 - 288, ISSN: 0013-5194, DOI: 10.1049/el:20000266. 11. Filanovsky, I.M., " *Stokes polynomial filters*", 2012 IEEE 55th Int. Midwest Symposium on Circuits and Systems (MWSCAS), Aug. 2012, pp. 734 - 737, ISSN: 1548-3746, E-ISBN : 978-1-4673-2525-7, Print ISBN: 978-1-4673-2526-4.
v	**4**	The paper: (**5.c.5**) V. B. Litovski, "*Synthesis of monotonic passband sharp cut-off filters with constant group delay response*", IEEE Trans. on Circuits and Systems, Vol. CAS-26, pp. 579-602, August 1979, was cited in: 1. In the paper: S. Sadughi, and H.K. Kim, "*An approximation procedure for selective linear phase filters*", IEEE Trans. on Circuits and Systems, Vol. CAS-34, No. 8, 1987, pp. 967-969. It is written: "**The second example is a filter of order 8 with two finite transmission zeroes and one pair of complex zeroes. It is designed for comparison with the design example given by Litovski** [7]. Under [7] the above is cited. 2. In the paper: Pang, K.K. and Kirton, P.A., *"Optimum flat delay filter characteristics***",** Int. J. of Circuit Theory and Applications, Vol. 10, No. 4, pp. 361 – 375. 3. In the Master Thesis: Sandhu, A.S., "*Generation of 2-D analog and digital lowpass, highpass and bandpass filters with monotonic amplitude-frequency response*", Concordia Uni., Faculty of Engineering and Computer Science, Electrical and

		Computer Engineering, Montreal, Canada, 2005. 4. Schwedersky, C., and Filho, S.N., "Uma Nova Função de Aproximação Least Square com Zeros Imaginários Obtidos por Otimização", XXVII Simpósio Brasileiro de Telecomunicações – SBrT 2009, Sept-Oct. 2009, Blumenau, SC, Brasil.
vi	**2**	The paper: (**5.c.8**) Milovanović, D., Litovski, V., *"Fault Models Of CMOS Transmission Gate"*, Int. J. of Electronics, ISSN 0020-7217, Vol. 71, No. 4, May, 1991, pp. 675-683, was cited: 1. In the paper: Liao, W., Tian, F., and Liu, J., "*Efficient fault diagnosis method in nonlinear circuits based on neural network*", Computer Engineering and Applications, Vol. 45, No. 19, 2009, pp. 228-231. 2. Wang Cheng "*Research on Analog Circuit Fault Diagnosis Based on Neural Network*" Microelectronics and Computers, 2010, No.5, pp. 125-128,
vii	**35**	The paper: (**5.c.10**) V.B. Litovski, J. Radjenović, Ž.M. Mrčarica, and S. Milenković, "*MOS transistor modelling using neural networks*", Electronic Letters, Vol. 28, No. 18, 1992, pp. 1766-1768 was cited 1. In the paper: Shahul Hameed, T.A., Baiju, M.R. and Predeep, P., "Organic Light Emitting Diodes: A Review on Device Physics, and Modeling using Artificial Neural Networks", NIT Calicut Research Review, December 2009, pp. 44-53,It is written: "**This new application of the artificial neural network (ANN) is first proposed by Litovski et al., [21] in 1992. Ever since, very few studies have been reported in black box modeling of microelectronic devices using ANN**." One comes to the same conclusion from: 2. Wang, F., and Zhang, Q.-j., "*Knowledge-based Neural Models for Microwave Design*", IEEE Trans. on MTT, Vol. 45, No. 12, Dec. 1997, pp. 2333-2343, is written: "It has been applied to efficient modelling microwave components, e.g., microstrip interconnections [1]-[3], vias [2], spiral inductors [4], FET devices [5], [6]; ...." 3. Wang, F. et all., "*Neural network structures and training algorithms for microwave applications*", Int. J. RF and Microwave CAE, Vol. 9, pp. 216-249, 1999, 4. Wang, B.-Z., "*Artificial neural network models for coaxial to waveguide adapters*" Int. J. of Infrared and Millimeter Waves, Vol. 20., No. 1, 1999, pp. 125-136.

5. Devabhaktuni, V., et all., "*Neural networks for microwave modelling: model development issues and nonlinear techniques*", Int. J. RF and Microwave CAE, Vol. 11, pp. 4-21, 2001. (invited review paper).
6. Watson, P.M.; Gupta, K.C., "*EM-ANN models for microstrip vias and interconnects in dataset circuits*", IEEE Trans. on Microwave Theory and Techniques, Vol. 44, No. 12, Dec. 1996, pp.2495 – 2503.
7. Jianjun Xu; Yagoub, M.C.E.; Runtao Ding; Qi Jun Zhang, "*Exact adjoint sensitivity analysis for neural-based microwave modeling and design*", IEEE Transactions on Microwave Theory and Techniques, Vol. 51, No. 1, Jan. 2003, pp. 226 – 237. 10.1109/TMTT.2002.806910
8. Hammouda, H.B., Mhiri, M., Gafsi, Z., and Besbes, B., "*Neural-Based Models of Semiconductor Devices for SPICE Simulator*", American J. of Applied Sciences, Vol. 5, No. 4, pp. 385-391, 2008. ISSN 1546-9239
9. In the MsSc thesis: Homayun, F., "*Development of A Library of Neural Models for Microstrip Line Components for High Frequency Circuit Design*", Ottawa-Carleton Institute for Electrical Engineering, Dep. of Electronics, Carleton University, Ottawa, Ontario KI S SB6, Canada, http://www.collectionscanada.ca/obj/s4/f2/dsk1/tape8/PQDD_0027/MQ52389.pdf.
9. In the MsSc thesis: Xi, C., "*Optimization Approaches to the Training of Neural Networks with RFtMicrowave Applications*", Ottawa-Carleton Institute for Electrical and Computer Engineering, Dept of Electronics, Carleton University, Ottawa, Ontario Kl S SB6,Canada, 1999 http://www.collectionscanada.ca/obj/s4/f2/dsk1/tape8/PQDD_0018/MQ48465.pdf
10. Wang, F., Devabhaktuni, V.K., Zhang, Q.-J., "*A hierarchical neural network approach to the development of a library of neural models for microwave design*", IEEE Transactions on Microwave Theory and Techniques**,** Volume 46, Issue 12 PART 2, 1998, pp. 2391-2403**.**
11. Tong, Q., Zou, X., and Tong, H., "MOSFET Life Model and NOME Distribution", http://public.whut.edu.cn/slx/English/HongKongConference/MOSFET.pdf
12. Tong, Q., Zou, X., Tong, H., and Liu, T., "Parameter Estimate by Incomplete Neural Network for MOSFET Life Model with NOME Distribution", Proc. of the Third Int. Conf. on Natural

Computation (ICNC 2007), Vol. III, 2007, pp. 318-322.
13. Wang, F., Devabhaktuni, V. K., Xi, C, Zhang, Q.-J., "*Neural Network Structures and Training Algorithms for RF and Microwave Applications*", Int. J. RF and Microwave CAE, No. 9, pp. 216-240, 1999, John Wiley & Sons, Inc.
14. Milovanović, B., et all., "Efficient Neural Models for Electromagnetic Field Characterisation – Application in RF Communications", Microwave Review, ISSN 14505835,Vol. 12, No. 1, June, 2006, pp. 31-35.
15. Kabir, H., Lei Zhang, Ming Yu, Aaen, P., Wood, J., Qi-Jun Zhang, "*Smart Modeling of Microwave Devices*", IEEE Microwave Magazine, May 2010, Vol. 11, No. 3, pp. 105 - 118, ISSN: 1527-3342.
16. Burniston, J.; Curtis, K.M., "A hybrid neural network/rule based architecture for diphone speech synthesis", Proc. of the 1994 Int. Symp. on Speech, Image Processing and Neural Networks, 1994. Proc., ISSIPNN '94, Hong Kong, April 1994, pp. 323 - 326 vol.1.
17. Izadian, M., Farokhi, F., and Fallahzadeh, M.R., "MOSFET simulation using neuro-fuzzy network", 2010 Second Pacific-Asia Conf. on Circuits,Communications and System (PACCS), 1-2 Aug. 2010, pp. 483 – 486, Beijing, China, Print ISBN: 978-1-4244-7969-6
18. Shahul Hameed.Ta, P. Predeep, and M.R.Baiju, "A Novel Modeling and Simulation Approach for Organic Light Emitting Diodes", Int. J. of Simulation Systems, Science & Technology, IJSSST, Vol. 11, No. 4, 2009, pp. 12-16, ISSN: 1473-804x online, 1473-8031.
19. Gupta, K.C., "ANN and Knowledge-Based Approaches for Microwave Design", pp 389-396, in: Das, N.K., and Bertoni, H.L., editors," Directions for the Next Generation of MMIC Devices and Systems", Polytechnic University Brooklyn, NY 11201, 1999.
http://www.dtic.mil/cgibin/GetTRDoc?AD=ADA365100#page=386
20. Bark, M.H., and Negm, M. H., "Modeling and design of high-frequency structures using artificial neural networks and space mapping", Silicon-based millimeter-wave technology – Measurement, modelling and application, Advances in Imaging and Electron Physics, Vol. 174, ISSN 1076-5670, 2012, pp. 223-269.
21. Mareddy, L., Almalkawi, M., Vemuru, S., Bakr, M., and

Devabhaktuni, V., "*Trust region-based optimization of PKI neural models for RF/microwave devices*", Int. J. of RF and Microwave Computer-Aided Engineering. Doi: 10.1002/mmce. 20690, 5 Oct. 2012.

22. Bahubalindruni, P.G., Tavares, V.G., Barquinha, P., Duarte, C., de Oliveira, P. G., Martins, R., and Fortunato, E., "*Transparent Current Mirrors With a-GIZO TFTs: Neural Modeling, Simulation and Fabrication*", J. of Display Technology, Vol. 9, Issue 12, pp. 1001-1006 (2013)
23. Bahubalindruni, P.G., Tavares, V.G., Barquinha, P., Duarte, C., Cardoso, N., de Oliveira, P. G., Martins, R., and Fortunato, E.," *A-GIZO TFT neural modeling, circuit simulation and validation*", Solid-State Electronics, Volume 105, March 2015, Pages 30–36.
24. Shunlu Zhang, "*Parallel Computation Based Neural Network Approach for Parametric Modeling of Microwave Circuits and Devices* ", A thesis submitted to the Faculty of Graduate and Postdoctoral Affairs in partial fulfillment of the requirements for the degree of Master of Applied Science in Electrical and Computer Engineering Ottawa-Carleton Institute for Electrical and Computer Engineering Carleton University, Ottawa, Ontario, 2012.
25. Sayed Alireza Sadrossadat, M.A.Sc., "*Sensitivity-Analysis-Based Adjoint Neural Network Techniques for Nonlinear Applications*", A thesis submitted to the Faculty of Graduate and Postdoctoral Affairs in partial fulfillment of the degree requirements of Doctor of Philosophy. Ottawa-Carleton Institute forElectrical and Computer Engineering, Department of Electronics, Carleton University, Ottawa, Ontario, Canada, 2015.
26. Gore , C.C., "*Study of Machine Learning algorithms for their use in Semiconductor Device Model Development*", A thesis submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the Degree of Master of Science Electrical and Electronics Engineering Raleigh, North Carolina, 2015.
27. Chie-In Lee , Yan-Ting Lin, Wei-Cheng, Lin, "*Improved artificial neural network RF noise model for MOSFETs operating in avalanche region*", Electronics Letters, 2 pp., DOI: 10.1049/el.2015.1607 , Online ISSN 1350-911X, Available online: 21 December 2015.

28. Bahubalindruni, G. , Tavares, V.G. ; Barquinha, P. ; Duarte, C., "*Basic analog circuits with a-GIZO thin-film transistors: Modeling and simulation*", 2012 IEEE Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Sept. 2012, pp. 261 – 264, Seville, Spain,DOI:10.1109/SMACD.2012. 6339389.
29. Bahubalindruni, G., Tavares, V.G., Duarte, C., Cardoso, N., "*Transparent Current Mirrors Using a-GIZO TFTs: Simulation with RBF Models and Fabrication*", 16th IEEE Int. Conf. on Computer Modelling and Simulation (UKSim), 2014 UKSim-AMSS, Cambridge, UK,March 2014, pp. 582-586, DOI: 10.1109/UKSim.2014.98.
30. Tuntas, R., " *The Modeling of Semiconductor Circuit Elements by Using Artificial Neural Networks*", J. of The Institute of Natural & Applied Sciences, Vol. 19, No. 1-2, pp. 48-53, 2014.
31. Zhang, S., "*Parallel Computation Based Neural Network Approach for Parametric Modeling of Microwave Circuits and Devices*", A thesis submitted to the Faculty of Graduate and Postdoctoral Affairs in partial fulfillment of the requirements for the degree of Master of Applied Science in Electrical and Computer Eng., Ottawa-Carleton Inst. for Electrical and Computer Eng., Carleton Uni., Ottawa, Ontario, 2012.
32. Zhang, J., Lv, Y, Chang, S., Wang, H., He, J., Huang, Q., "*Prior knowledge input neural network method for GFET description*", J. of Computational Electronics, ISSN: 1569-8025, Vol. 15, 2016, pp 1–8.
33. Goudarzi, S., Hassan, W. H., Hashim, A.-H. A., Soleymani, S. A., Anisi, M. H., Zakaria, O. M. "*A Novel RSSI Prediction Using Imperialist Competition Algorithm (ICA), Radial Basis Function (RBF) and Firefly Algorithm (FFA) in Wireless Networks*", PLOS one. , 2016, Vol. 11, No. 7, p.e 0151355.
34. Feng, F., "*Parametric Modeling of EM Behaviors of Microwave Components Using Combined Neural Networks and Pole-Residue Transfer Functions*", A PhD thesis submitted to the Faculty of Graduate and Postdoctoral Affairs, School of Microelectronics Tianjin University, Tianjin, China; Ottawa-Carleton Institute for Electrical and Computer Engineering Carleton University, Ottawa, Ontario, Canada, ©2017.
35. Chie-In Lee, Yan-Ting Lin & Wei-Cheng Lin, "*An improved large-signal model by artificial neural network for the MOSFETs operating in the breakdown region*", J. of

		Electromagnetic Waves and Applications, Vol. 31, 2017, Issue 11-12, pp. 1160-1166.
viii	**1**	The paper: (**5.c.13**) Litovski, V., Mrčarica, Ž., *"Macromodeling With Spice's Nonlinear Controlled Sources"*, IEEE Circuits and Devices Magazine, Vol. 9, No. 6, November, 1993, pp. 14-17,51, is cited in: 1. In the book: Graham F. Carey, G.F., "*Circuit, Device, and Process Simulation: Mathematical and Numerical Aspects*", John Wiley & Sons, Inc. New York, NY, USA, 1996, ISBN: 0471960195
ix	**7**	The paper: (**5.c.14**) Milovanović, D. B., and Litovski, V. M., "*Fault models of CMOS Circuits*", Microelectrinics Reliability, Vol. 34, No. 5, pp. 883-896, 1994, is cited in: 1. In the paper: Ževma, A., and Zajc, B., "*Functionality fault model: a basis for technology-specific test generation*", Microelectronics Reliability", Vol. 38, No. 4, pp. 579-604, 1998, is written: "Although it is becoming evident that **the most accurate fault modelling in digital circuits implemented in CMOS technology is at the transistor level [4-6]** the simplicity ....". Under [4] the above is cited. 2. In the paper: Sedaghat, R., Kunchwar, M., Abedi, R., and Javaheri, R., "*Transistor-level to gate-level comprehensive fault synthesis for n-input primitive gates*" Microelectronics and Reliability**,** Volume 46, Issue 12, December 2006, Pages 2149-2158 3. In the paper: Zemva, A., and Zajc, B., "*Test generation for technology-specific multi-faults based on detectable perturbations*", Microelectronics Reliability, Vol. 45, No. 1, Jan. 2005, pp. 163-173. 4. In the editorial: "Zorian, Y., AT&T Bell Laboratories, Hlavicka, J., Czech Technical university, "*East Meets West*", Guest Editors' Introduction, IEEE Design and Test of Computers, Spring 1996 (Vol. 13, No. 1), pp. 5-7, in the following way: **D.P. Milovanovic and V.B. Litovski from the University of Nis (Yugoslavia) search for modeling procedures and fault models for BiCMOS circuits. Simulation results analyze fault mechanisms and behavior.** 5. In the paper: Liao, W., Tian, F., and Liu, J., "Efficient fault diagnosis method in nonlinear circuits based on neural network", Computer Engineering and Applications, Vol. 45,

		No.19, 2009, pp. 228-231. 6. In the Master thesis: Abedi, R., "*Synthesis of Classical and Non-Classical CMOS Transistor Fault Models Mapped to Gate-Level for Reconfigurable Hardware-Based Fault Injection*", Ryerson University, Toronto, Ontario, Canada, 2005. 7. Liao, W., "*Research on Analog Circuit Fault Diagnosis Based on Neural Network*", Microelectronics and Computers, 2010, No.5, pp. 125-128.
x	**1**	The paper: (**5.c.17**) Petković, P., Stojilković, S., and Litovski, V., "*Factorization algorithm for symbolic circuits analysis*", IEE Electronic Letters, Vol. 31, No. 13, pp. 1026-1027, June 1995, was cited in: 1. Topa, M., et all., "*Postprocessing techniques for approximate symbolic network functions of complex analog integrated blocks*", Proc. ECCTD' 97, Budapest, September 1997, pp. 1464-1467, is written: "Next it is counted how many times each symbol occurs in a term. **This is performed in much the same way as described in [6]",** as [6], the above was cited.
xi	**1**	The paper: (**5.c.19**) Radjenović-Mrčarica, J., Mrčarica, Ž., Detter, H., Brenner, W., and Litovski, V., "*Neural Network Visual Recognition Applied to Microelectromechanical part Assembly*", VDE Verlag Berlin und Offenbach London, 1996, pp. 325-328. 1. In the project application: The Technical University of Vienna, "*Handhabung und Montage mikromechanischer Bauelemente*", lead by Dr. Brenner, in the list of important publications is cited: h*ttp://www.tuwien.ac.at/ histu/inst/fp/ 0003580107.html.*
xii	**1**	The paper: (**5.c.20**) Petković, P., Milovanović, D., Litovski, V., *"Symbolic Fault Modelling And Test Generation Of MOS Circuits"*, Microelectronics and Reliability, Vol. 37, No. 1, 1997, pp. 137-157.Was cited in: 1. Žemva, A., and Zajc, B., "Test generation for technology-specific multi-faults based on detectable perturbations", Microelectronics Reliability, Vol. 45, No. 1, Jan. 2005, pp. 163-173.
xiii	**3**	The paper: (**5.c.21**) Mrčarica, Ž., Litovski, V. and Detter, H., "*Modeling and simulation of microsystems using hardware description language*", Microsystem Technology, Vol. 3, No. 2, 1997, pp. 80-85, was cited in: 1. In the invited paper: Senturia, S. D., "*CAD challanges for Microsensors, Microactuators, and Microsystems*", invited paper, Proceedings of the IEEE, Vol. 86, No. 8, August 1998., pp. 1611-

		1626, , where was written: **"And using so-called "hardware description languages" [178]-[180], such models can be readily inserted into circuit simulators for behavioral simulation at the system level, including feedback effects around nonlinear devices."** 2. In the PhD thesis: Wuzhong, L. W., "*Model Order Reduction Techniques in Microelectromechanics*", Department of Mechanical Engineering National University Of Singapore, 2004. 3. In the master thesis: Abu Bakar, A. R., "*Modelling of mixed physical-domain system*", Uni. of Southampton, School of Electronics and Computer Science, UK, 2010, 133pp.
xiv	**4**	The paper: (**5.c.22**) Litovski, V., Mrčarica, Ž., Ilić, T., *"Simulation Of Non-Linear Magnetic Circuits Modelled Using Artificial Neural Network"*, J. Simulation Practice and Theory, ISSN: 1569-190X, Vol. 5, No. 6, 1997, pp. 553-570, was cited in 1. "Magnetic Resource Directory", http*://www.magnetsmagnetic.info/magneticcircuits/* 2. In the paper: Sutanto, J., Setia, R., Papania, A., May, G.S., Hesketh, P.J., and Berthelot, Y.H., "*Using neural networks to model an electromagnetic-actuated microactuator*", J. Micro/Nanolith. MEMS MOEMS 6, 12 March 2007, 013011, doi:10.1117/1.2712864. 3. In the paper: Nouir, Z., Sayrac, B., Fourestie, B., Tabbara, W., and Brouaye, F., "*Generalization Capabilities Enhancement of a Learning System by Fuzzy Space Clustering* ", J. of Communications, Vol. 2, No. 6, Nov. 2007, pp. 30-37. 4. In the paper: Mohamad Ghazali B. Ameer Amsa, A. M. Aibinu, M. J. E. Salami, "*A Novel Hybrid Artificial Intelligence Technique for Colpitts Oscillator Design*", J. of Control, Automation and Electrical Systems, February 2014, Vol. 25, Issue 1, pp 10-21.
xv	1	The paper: (**5.c.24**) Litovski, V., Dimić, Ž., Damnjanović, M., Mrčarica*, Ž., "Electronic Circuit Simulation In A Mixed-Language Environment*", Microelectronics Journal, Vol. 29, No. 8, 1998, pp. 553-558, was cited: 1. In the US patent: Meyer, S. J., "*Mixed signal simulation*", Application Number: EP20010954620, Patent EP1305765, Publication Date: 05/02/2003.
xvi	**2**	The paper: (**5.c.25**) Maksimović, D., and Litovski, V., "*Tuning logic simulator for timing simulation*", Electronic Letters, Vol. 35, No. 10.

		May 1999, p. 800-802, was cited in: 1. The curriculum: The University in Linköping, Sweden, Department of physiscs, tehnolgy, measurement, biology and chemistry, at the postgraduate level performes teaching in design automation in electronics for design in physics. Within the subject logic simulation it is recommended the paper: (*http://www.ifm.liu.se/čperla/EDA_Course/ topics.html).* 2. In the paper: Zdraveski, Z., Dimitrovski, D., and Trajanov, D., "*HDL IP Cores System as an Online Testbench Provider*", Proc. of the Small Systems Simulation Symposium, SSSS'2014, Niš, Serbia, 108-112.
xvii	**23**	The paper: (**5.c.26**) Mrčarica, Ž., Ilić, T., and Litovski, V., "*Time-Domain Analysis of Nonlinear Switched networks with internally controlled switches*", IEEE Trans. on Circuits and Systems - I: Fundamental Theory and Applications, ISSN: 1057-7122, Vol. 46, No. 3, March 1999, pp. 373-378, was cited: 1. In the paper: Pietrenko, W., Janke, W., and Kazimierczuk, M., "*Application of Semianalytical Recursive Convolution Algorithms for Large-Signal Time-Domain Simulation of Switched-Mode Power Converters*", IEEE Trans. on Circuits and Systems - I: Fundamental Theory and Applications, Vol. 48, No. 10, October 2001, pp. 1246-1252, is written: "**The difficulties of handling the Dirac delta impulses and the methods to overcome them are discussed in [2]-[5]**. The reference [5] is above. 2. In the paper: Demir, Y, and Köksal, M., "*State space suitable modelling of power semiconductors with ideal switches, resistors, constant voltage and current sources*", Electronic Engineering (Archiv fur Elektrotechnik), Vol. 86, No. 3, Feb. 2004, pp. 135-145, kao i u 3. In the paper: Herdem, S., and Köksal, M., "*A fast algorithm to compute the steady-state solution of nonlinear circuits by piecewise linearization*", Computers & Electrical Engineering, Vol. 28, No. 2, March 2002, pp. 91-101, 4. In the apaper: Cheong, S.V., Chung, S.H., Ioinovici, A., **"***Duty-cycle control boosts DC-DC converters*", Circuits and Devices Magazine, IEEE**,** Mar. 1993, Vol. 9, No. 2, pp. 36-37, ISSN: 8755-3996. 5. In the paper: Francisco del Águila López, Pere Palà Schönwälder, Jordi Bonet Dalmau y Rosa Giralt Mas, "*Técnica de Análisis de Circuitos Conmutados no Lineales con*

		Topologías Independientes", http://w3.iec.csic.es/ursi/articulos_coruna_2003/actas_pdf/SESION%202/S2.%20Aula%202.2/1499%20-%20TECNICA%20DE%20ANALISIS.pdf is written : **Para superar estas dificultades existen algunas técnicas que utilizan modelos específicos de conmutadores** [3], where [3] is above. 6. In the paper: F. Del Aguila Lopez, P. Pal Schoenwalder, and J. Bonet Dalmau, Mas, R.G, "*A discrete-time technique for the steady state analysis of nonlinear switched circuits with inconsistent initial conditions*", The 2001 IEEE Int. Symposium on Circuits and Systems, 2001, ISCAS 2001, Volume 3, 6-9 May 2001, pp. 357 – 360. 7. In the paper: del-Aguila-Lopez, F.; Pala-Schonwalder, P.; Molina-Gaudo, P.; Mediano-Heredia, A.; "*A Discrete-Time Technique for the Steady-State Analysis of Nonlinear Class-E Amplifiers*"**,** IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol. 54, No. 6, June 2007, pp. 1358 - 1366. 8. In the paper: Herdem, S. and Köksal, K., "*Fast algorithm to compute the steady-state solution of nonlinear circuits by piecewise linearization*", Computers & Electrical Engineering , Elsevier, Volume 28, Issue 2 , March 2002, pp. 91-101. 9. In the paper: Luhuai MA Xi Zhao Wei Yin, "*Piecewise linear analysis of network switching nodes Equations*", J. of XI 'AN Jiaotong University, 2002, Vol. 36, No.6, pp.559 – 563. 10. In the paper: Acciani, G., Chiarantoni, E., Fornarelli, G., and Vergura, S., "*An Homotopy Function for Transient Analysis of Switching Circuits*", IEEE ISIE 2005, June 2005, Dubrovnik, Croatia, pp. 595-600. 11. In the paper: Welsch, G. Brachtendorf, P.G. Sabelhaus, C. Laur, R. "*Minimization of the error in the calculation of the steady state byshooting methods*", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Oct. 2001, Vol. 48, No. 10, pp. 1252-1257, ISSN: 1057-7122. 12. In the paper: Wang, S, et all., "*An improved V-A characteristics of switches and its application in coupled field-circuit simulation of permanent magnet brushless DC motor*", The 4th Int. Power Electronics and Motion Control Conf., IPEMC 2004, Aug. 2004, Vol. 2, pp. 1013- 1017, ISBN: 7-5605-1869-9. 13. In the paper: del Aguila, F.; Pala, P.; Bonet, J.; Xavier

		Moncunill, F.; Giralt, R., "*Analysis of Nonlinear Switched Circuits with Different State Variables in Each Topology*", 14th IEEE Int. Conf. on Electronics, Circuits and Systems, 2007, ICECS 2007, Dec. 2007, pp. 1039 – 1042 14. In the paper: Yin, Youwei; Zhao, Luhuai; Ma, Xikui**, "***Novel Method for the Analysis of Piece-Wise Linear Switched Networks Based on Differential Nodal Equations*", J. of XI'AN Jiaotong University 2002, Vol.36, No.6 pp. 559-563. 15. In the paper: Liao, W., Tian, F., and Liu, J., "*Efficient fault diagnosis method in nonlinear circuits based on neural network*", Computer Engineering and Applications, Vol. 45, No.19, 2009, pp. 228-231 16. In the paper: Gorecki, K. Zarebski, J. , "*The method of a fast electrothermal transient analysis of a buck converter*", 15th IEEE Int. Conf. on Electronics, Circuits and Systems, ICECS 2008. Aug. / Sept. 2008, pp. 630 – 633, St. ISBN: 978-1-4244-2181-7. 17. In the paper: Yildiz, A.B., Cinar, M.A., "*Time-Domain Analysis of Circuits with Ideal Switches by Nodal Equations*", Int. Conf. on Power Electronics and Drives Systems, 2005. PEDS 2005. Kuala Lumpur, Malezia, Nov.-Dec. 2005, pp. 1046 – 1050, Print ISBN**:** 0-7803-9296-5. 18. In the paper: Wojciechowski, J., Modzelewski, J., Ogrodzki, J., Opalski, L., Zamłyński, K., "*Computer-Aided Multi-Layer Design of Switch-Mode Power Circuits*", Intl J. of Electronics and Telecommunications, September 2010, Vol. 56, No. 3, pp. 307-318. 19. In the paper: Gorecki, K.; Zarebski, J.; "*The method of a fast electrothermal transient analysis of single-inductance dc-dc converters*", IEEE Trans. on Power Electronics, Vol. 27, No. 99, pp. 1 - 1, ISSN: 0885-8993. 20. In the paper: Yildiz, A.B., "*A MNA-Based Unified Ideal Switch Model for Analysis of Switching Circuits*", J. of Circuits, Systems and Computers, Vol. 22, Issue 06, July 2013, Article Number: 1350046. 21. Zhao, ??, "*Exponential Attenuation Power Supply Model and Simulation of Switching Process in Switching Networks*" J. of System Simulation, Vol. 16, No. 5, 2004, https://translate.google.rs/translate?hl=en&sl=zh-CN&u=http://d.wanfangdata.com.cn/periodical/xtfzxb200405064&prev=search 22. Luhuai, Z., and Shuhong, W, "*Single voltage current equations of ideal switches and its application in rime-domain*

		analysis of electric circuits", J. of Xi'an Jiaotong University, Vol 36, No. 10, 2002. 23. Liao, W., Tian, F., Liu, J.-g, "*Efficient fault diagnosis method in nonlinear circuits based neural network*", Computer Engineering and Applications, Vol. 45, No. 19, 2009, pp. 228-231.
xviii	**2**	The paper: (**5.c.27**) Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., Litovski, V., "*Transient Electro-Thermal Simulation Of Microsystems With Space-Continuous Thermal Models In Analogue Behavioural Simulator*", Microelectronics and Reliability, Vol. 40, No. 3, March 2000, pp. 507-516, was cited: 1. In the paper: Liu, G., Wang, A., Jiang, T., Jiao, J., Jang, J.B., „*Effects of environmental temperature on the performance of a micromachined gyroscope*", Microsystem Technologies (Springer), Volume 14, Number 2 / February, 2008, pp. 199-204. 2. Guo Zhanshe, Cheng Fucheng, Li Boyu, Cao Le, Lu Chao, Song Ke, "Research development of silicon MEMS gyroscopes: a review", Microsystem Technologies, October 2015, Vol. 21, Issue 10, pp. 2053–2066 .
xix	**1**	The paper: (**5.c.28**) Ilić, T., Litovski, V., Litovski, I., Stojilković, S., "*Computationally Efficient Large-Change Statical Analysis Of Linear Electronic Circuits*", Microelectronics and Reliability, Vol. 40, 2000, pp. 1023-38, was cited: 1. In the paper: Grasso, F., Manetti, S., and Maria Cristina, P.M., "*A symbolic approach to design centering of analog circuits*", Microelectronics & Reliability, 2007, Vol. 47, No. 8, pp. 1288-1295, ISSN: 0026-2714.
xx	**1**	The paper: (**5.c.30**) M. Jakovljević, P. A. Fotiu, Ž. Mrčarica, V. Litovski, H. Detter, "*Electro-thermal Simulation of Microsystems with mixed abstracttion modeling*", Microelectronics Reliability Vol. 41, No. 6, 2001, pp. 823-835. 1. In the paper: Nagy, G., Horváth, G., and Poppe, P., "*Consideration of Thermal Effects in Logic Simulation*", Proc. of the THERMINIC 2008, 24-26 September 2008, Rome, Italy, pp. 229-234, EDA Publishing, ISBN: 978-2-35500-008-9 229.
xxi	**8**	The paper: (**5.c.34**) Milojković, J.B. and Litovski V.B., "*Eco-Design in Electronics – The State of the Art*," Facta Universitatais,

		Series: Working and Living Environmental Protection, Vol. 2, No 2, 2002, pp. 87 – 100, was cited: 1. In the paper: Parsons, David (2006) *'The Environmental Impact of Electronics and Its Incorporation into the Curriculum*.' in: 17th Annual Conf. of the Australasian Association for Engineering Education, 10-13 December 2006, Auckland, New Zealand, 2. In the PhD thesis: *Munitlak, Đ., "*Model upravljačkog sistema u zaštiti životne sredine i održivog korišćenja resursa*», Doktorska disertacija, Asocijacija centara za interdisciplinarne i multidisciplinarne studije i sitraživanja, Centar za inžinjerstvo za zaštitu životne sredine, Novi Sad, 2007. 3. In the paper: Amitava Bandyopadhyay, "*A regulatory approach for e-waste management: a cross-national review of current practice and policy with an assessment and policy recommendation for the Indian perspective***"**, Int. J. of Environment and Waste Management, Volume 2, Number 1-2 / 2008, pp. 139 – 186, 4. In the paper: Nnorom, I.C., et all., "*Achieving Resource Conservation in Electronic Waste Management: A Review of options Available to Developing Countries*", J. of Applied Sciences, ISBN 1812-5654, Vol. 20, No. 7, 2007, pp. 2918-2933. 5. In the Master thesis: Chongwatpol, J., "*Analysis of waste electrical and electronic equipment (WEEE) in Thailand and implementation of risk management plan to comply with future WEEE regulations*", MSc thesis, The Graduate School, University of South Wisconsin, USA, 2004. 6. In the Master thesis: da Fonseca, C.G.P., "*Ecodesign e a reutilização de computadores*", Master Thesis, Faculdade de Engenharia da Universidade do Porto, Portugal, 2007. 7. In the Master thesis: Vasudev, J., "*The Post-Consumptive Residues of Information Technology: E-waste Management and Disposal in Bangalore and Chennai, India*", A Thesis Submitted in Partial Fulfillment for the Award of M.Tech. In Information Technology, Int. Institute of Information Technology, Bangalore, India, 2007. 8. In the paper: Abdalla, H.S., and Ebeid, M.A., "*A holistic approach for sustainable product design*", Proc. Of the Global Product Development: 20th Cirp Design Conf. 2010, Edited by Bernard, A., Nantes, France, April 2010, pp. 329-338.

xxii	**2**	The paper: (**5.c.36**) Maksimović, D.M., Litovski, V.B., "*Logic simulation methods for longest path delay estimation*", IEE Proceedings: Computers and Digital Techniques, Vol. 149, No. 2, 2002, pp. 53-59, was cited: 1. In the paper: Minjie, M., Zheying, L., Guangyu, J., "*Study on analyzing and modeling of delay activity for digital circuit*", ASICON 2005, Proc. of the 6th Int. Conf. on ASIC, Vol. 2, 2005, Article number 1611420, pp. 681-684**,** 2. Zheying, L., Minjie, M., and Zhi, L., "*Study on Detecting of Competition Phenomena of Signal for Logic Combinational Circuit*", 8th Int. Conf. on Signal Processing, 2006, Beijing, ICSP, Vo. 4, 2007, Article number 4129831, Print ISBN: 0-7803-9736-3.
xxiii	**1**	The paper: (**5.c.37**) Savić, M., Litovski, V., "*Frequency Domain Electronic Circuit Analysis in an Object Oriented Environment*", Proc. of the 11th Int. Scientific and Appl. Sci. Conf. of Electronics, ET2002, Sep., 2002, Sozopol, 2002. Vol. 2, pp. 65-70, was cited: 1. On the web site Pdfgeni.com, within the subject "electronic circuit analysis and design" http://www.pdfgeni.com/book/electronic-circuit-analysis-and-design-pdf.html, the above paper is offered.
xxiv	**8**	The paper: (**5.c.38**) Andrejević, M., Litovski, V., "*Electronic circuits modeling using artificial neural network**s***", J. of Automatic Control, University of Belgrade, doi: 10.2298/JAC0301031A, Vol. 13, No. 1, 2003, pp. 31-37, was cited: 1. In the paper: Hayati, M., Rezaei, A., Seifi, M., and Naderi, A., "*Modeling and simulation of combinational CMOS logic circuits by ANFIS*", Microelectronics Journal, ISSN: 0026-2692, Vol. 41, No. 7, July 2010, pp. 381-387, 2. In the paper: Izadian, M., Farokhi, F., and Fallahzadeh, M.R., "*MOSFET simulation using neuro-fuzzy network*", paper appears in: 2010 Second Pacific-Asia Conf. on Circuits, Communications and System (PACCS), 1-2 Aug. 2010, pp. 483 – 486, Beijing, China, Print ISBN: 978-1-4244-7969-6. 3. In the paper: Tuntaş, R., "*IDEAS The Modelling Technique Based on Neuro-Fuzzy Structure for Chaotic Rossler System*", Chaos, Complexity and Leadership 2012, Springer Proceedings in Complexity 2014, ISBN-10: 9400773617 , ISBN-13: 978-9400773615, pp 177-181. 4. In the paper: Sharma, D. P., "*Neural Network Simulation of Digital Circuits*", Int. J. of Computer Applications, ISSN for

		IJCA Digital Library is 0975 - 8887, Oct. 2013, Vol. 79, p7-13. 7p. 5. Bhatia, V., Pandey, N., and Bhattacharyya, A., "*Modelling and Design of Inverter Threshold Quantization Based Current Comparator using Artificial Neural Networks*", Int. J. of Electrical and Computer Eng. (IJECE), Vol. 6, No. 1, February 2016, pp. 320-329. 6. Tuntaş, R., "Predict and analysis of the full -wave rectifier circuit with Fuzzy Modeling technique based on performances of different membership functions", Energy Education Science and Technology, Part A: Energy Science and Research 2012, Special Issue, pp. 539-548. 7. Tuntaş, R., "The modelling and analysis of nonlinear systems using a new expert system approach ", Iranian Journal of Science & Technology, IJST (2014) 38A3 (Special issue-Mathematics), pp. 365-372. 8. Bhatia, V., Gupta, K., Batra, N., Pandey, N., "Modelling a simple current to voltage converter using ANN", IEEE Int. Conf. on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), July 2016, **DOI:** 10.1109/ICPEICES.2016.7853224, Delhi, India.
xxv	**4**	The paper: (**5.c.39**) Litovski, V. B., Andrejević, M., Petković, P., Damper, R., "*ANN Application to Modelling of the D/A and A/D Interface for Mixed-Mode Behavioural Simulation*", J. of Circuits, Systems and Computers, Vol. 13, No. 1, February 2004, pp. 181-192, was cited: 1. In the patent: Jones, K.D. (Hayward, CA, US), Sheffler, T. J. (San Francisco, CA, US), Mossawir, K. M. (Stanford, CA, US), Hong, Q. (San Jose, CA, US), Wong, P.(San Jose, CA, US), Jiang, J. (Stanford, CA, US), **«** *Mixed mode verifier* **»,** Number: United States Patent 7360187 2. In the paper: Čeperić, V., Barić, A., "*A brief overview of the black-box behavioural modelling of electronic circuits for transient simulations*," *MIPRO, 2012 Proceedings of the 35th Int. Convention*, pp.72, 77, 21-25 May 2012. 3. Zhongkai Ji, Jianguo Ma, and Oliver Faust, "*Formal And Model Driven Design Of A High Speed Data Transmission Channel*", J. of Circuits, Systems and Computers, Print ISSN: 0218-1266, Online ISSN: 1793-6454, Vol. 22, No. 10, 2013, Paper no. 1340038. 4. Ceperic, V., Gielen, G., Baric, A., "Black-Box Modelling of

		AC-DC Rectifiers for RFID Applications Using Support Vector Regression Machines", 2013 UKSim 15th Int. Conf. on Computer Modelling and Simulation (UKSim), April 2013, **DOI:** 10.1109/UKSim.2013.104, Cambridge, UK.
xxvi	**7**	The paper: (**5.c.40**) V. B. Litovski, I. V Litovski, and M. Zwolinski, "*Concurrent analogue fault simulation, the equation formulation aspect*", Int. J. of Circuit Theory and Applications, Vol. 32, No. 6, pp. 487-507, 2004, was cited in 1. The project application: "*Meeting the Design Challenges of Nano-CMOS Electronics*", at EPSRC (Electronics and physics research council), by the: Institute for Integrated Micro and Nano Systems (IMNS), School of Engineering and Electronics, Science and engineering at the University of Edinbrough. www.see.ed.ac.uk/~afm/tmp/eScience.pdf, as well as in the papers: 2. In the paper: Garczarczyk, Z.A. , "*Polynomial fault diagnosis of linear analog circuits*", 18th European Conf. on Circuit Theory and Design, 2007, ECCTD 2007, Seville, Aug. 2007, pp. 842-845, ISBN: 978-1-4244-1341-6, DOI: 10.1109/ ECCTD.2007.4529728. 3. In the paper: Izydorczyk, J., and Chojcan, J., "*High-order sensitivity invariants*", Int. J. of Circuit Theory and Applications, Vol. 39, No. 12, Dec. 2011, pp. 1285–1304. 4. In the habilitation: Mir, S., "*Conception Et Test Integre Des Dispositifs Analogiques, Mixtes Et Microsystemes*", L'habilitation A Diriger Des Recherches, s*pécialité :Microet NanoElectronique,*préparée au laboratoire TIMA, dans le cadre de l'Ecole Doctorale «Electronique, Electrotechnique, Automatique, Télécommunication, Signal», le 18 mai 2005, Grenoble, France. 5. In the PhD thesis: Bounceur, A., « *Plateforme CAO pour le test de circuits mixtes* », Institut national polytechnique de Grenoble, École Doctorale d'Électronique, d'Électrotechnique, d'Automatique et de Traitement du Signal, Grenoble, France, 2007. 6. Michel Morneau," *Methodes d'acceleration de la simulation analogique utilisee dans des applications necessitant des simulations multiples*", Library and Archives Canada = Bibliothèque et Archives Canada, 2007, ISBN 0494255625. 7. In the paper: Wenxin Yu, Yigang He , "*Analog Circuit Fault Diagnosis via Sensitivity Computation"* , Journal of Electronic

		Testing , February 2015, Volume 31, Issue 1, pp 119-122
xxvii	**2**	The paper: (**5.c.48**) V., Litovski, M., Savić, and Ž., Mrčarica, '*Electronic circuit simulation with ideal switches*', July 2005, HAIT J. of Science and Engineering B, pp. 476-495. 1. In the paper: Batard, C., Poitiers, F. and Machmoum, M., « *An Original Method to Simulate Diodes Rectifiers Behaviour with Matlab-Simulink Taking into Account Overlap Phenomenon*", IEEE Int. Symp. on Industrial Electronics, 2007. ISIE 2007. pp. 971-976, Vigo, Spain, ISBN: 978-1-4244-0755-2. 2. In the paper: Sheffler, T.J. "*Design of a Switch-Level Analog Model for Verilog*", IEEE Int. Behavioral Modeling and Simulation Workshop, BMAS 2008, September 2008, pp. 118-123, DOI 10.1109/ BMAS.2008.4751252
xxviii	**12**	The paper: (**5.c.49**) Milojković, J., and Litovski, V., "*Concepts of computer take-back for sustainable end-of-life*", Facta Universitatis, Series: Working and Living Environmental Protection, Vol. 2, No. 5, 2005, pp. 363-372, was cited: 1. In the paper: Osibanjo O., and Nnorom, I.C. **«***The challenge of electronic waste (e-waste) management in developing countries*", Waste Management & Research, Vol. 25, No. 6, 489-501, 2007, DOI: 10.1177/ 0734242X07082028, © 2007 Int. Solid Waste Association. 2. In the paper: Nnorom I.C., and Osibanjo, O. "*Overview of electronic waste (e-waste) management practices and legislations, and their poor applications in the developing countries*", Resources, Conservation and Recycling, Vol. 52, No. 6, April 2008, pp. 843-858, 3. In the paper: Osibanjo, O. and Nnorom, C. I., "*Material flows of mobile phones and accessories in Nigeria: Environmental implications and sound end-of-life management options*", Environmental Impact Assessment Review, Vol. 28, No. 2-3, Feb.-April 2008, pp. 198-213, 4. In the paper: Wagner, T. P., "*Shared responsibility for managing electronic waste: A case study of Maine, USA***",** Waste Management, Vol. 29, No. 12, Dec. 2009, pp. 3014-3021, 5. In the text: "Global E-waste Perspective and Management Approaches" on the page: http://redlink.blogfa.com/post-141.aspx 6. In the paper: Nnorom, I.C., Osibanjo, O., Okechukwu, K., Nkwachukwu O., and Chukwuma, R.C, "*Evaluation of Heavy Metal Release from the Disposal of Waste Computer Monitors at an Open Dump*", Int. J. of Environmental Science and

		Development, Vol. 1, No. 3, August 2010, pp. 228-233. ISSN: 2010-0264. 7. In the paper: Premalatha, M., Abbasi, Tabassum; Abbasi, Tasneem; and Abbasi, S. A., "*The generation, impact, and management of E-waste: State-of-the-art*", Critical Reviews in Environmental Science and Technology, Published online: 28 Aug 2013, Volume 44, Issue 4, 2014 ISSN 1064-3389 (Print), 1547-6537 (Online), DOI: 10.1080/ 10643389.2013.782171. 8. In the monograph chapter: Ward, A.L. and Sasco, A. "*Plastics Recycling and Women's Reproductive Health*" (in "*Our Chemical Selves: Gender, Toxics, and Environmental Health*", edited by Dayna Nadine Scott, Published by UBC Press, Vancouver,Canada, 2015,) pp. 253-285. 9. In the paper: Wei, L., Wang, S., Zuo, Q., Liang, S., Shen, S., and Zhao, C., "*Nano-hydroxyapatite alleviates the detrimental effects of heavy metals on plant growth and soil microbes in e-waste-contaminated soil*", Environmental Science Processes & Impacts, Vol. 18, No. 6, June 2016, pp. 641-770. 10. In the paper: M. Premalatha, Abbasi, T., Abbasi, S. A., "*The Generation, Impact, and Management of E-Waste: State of the Art*", Critical Reviews in Environmental Science and Technology, Vol. 44, No. 14, July 2014, pp. 1577-1678. 11. In the master thesis: Sunanda, M., "*Extended Producer Responsibility for Solar Photovoltaic panels: Practices and challenges for end-of-life management in Germany, Italy and Switzerland*", (2017) In IIIEE Theses IMEN56 20171. The Int. Institute for Industrial Environmental Economics, Lund University, Denmark. 12. Pathak, P., Srivastava, R.R., and Ojasvi, "*Assessment of legislation and practices for the sustainable management of waste electrical and electronic equipment in India*", Renewable and Sustainable Energy Reviews, Vol. 78, Oct. 2017, pp. 220-232.
xxix	**34**	The paper: (**5.c.51**) Litovski, V., Andrejević, M., and Zwolinski, M. "*Analog electronic circuit diagnosis based on ANNs* ", Microelectronics Reliability, Vol. 46, 2006, pp. 1382-1391, was cited: 1. In the paper: Petlenkov, E., Jutman, A., Nomm, S., and Ubar, R. „*Towards artificial intelligence based automatic adaptive response analyzer for high frequency analog BIST*",

		Proc. of 2008 IEEE Int. Conf. on Computational Intelligence for Measurement Systems and Applications, CIMSA 2008. July 2008, pp. 99-104, Istanbul, ISBN: 978-1-4244-2305-7, 2. In the paper: Jantos, P., Grzechca, D., Rutkowski, J., "*Global Parametric Fault Identification In Analog Electronic Circuits*", Metrology And Measurement Systems, Vol. XVI, No. 3, 2009, Paper No. M 0310. ISSN 0860-8229, www.metrology.pg.gda.pl. 3. In the paper: Kuczynski, A., and Ossowski, M., "*Circuit Fault Diagnosis Based on Wavelet Packet and Neural Network*", Proceedings of ISTET 2009, VXV Int. Symposium on Theoretical Engineering, Lübeck, Germany, June 2009, pp. 114-117. 4. In the paper: Jingyuan, T., Yibing, S., Longfu, Z., and Wei, Z. , "*Analog circuit fault diagnosis using Ada Boost and SVM*", Int. Conf. on Communications, Circuits and Systems, ICCCAS 2008, May 2008, pp. 1184 – 1187, Fujian, China, ISBN: 978-1-4244-2063-6. 5. In the paper: Zhang Rui, Yang Xuan-fang, "*Research of Analog Circuit Fault Diagnosis Based on Modified BP Neural Network*", Ordnance Industry Automation, Vol. 28, No. 9, Sep. 2009, pp. 71-73. 6. In the paper: Song Guo-ming, Wang Hou-jun, Jyang Shu-yan, and Liu Hong, "*Analog circuit fault identification approach based on wavelet analysis and hierarchical decision*", Application Research Of Computers, 2010, Vol. 27, No. 6, pp. 2057-2064. 7. In the paper: Hong, S., Jingyuan, T., Xiqu, C., Xiaohong, K., "*Analog circuit fault diagnosis combing wavelet packet with higher order statistics*", 2nd Int. Conf. on Signal Processing Systems (ICSPS), Dalian, China, July 2010, pp. V1-368 - V1-371, Print ISBN: 978-1-4244-6892-8. 8. In the paper: H. Luo, Y. Wang, H. Lin, and Y. Jiang, "*A New Optimal Test Node Selection Method for Analog Circuit*", J. of Electronic Testing, DOI: 10.1007/s10836-011-5274-z, 9. In the paper: Sheikhan, M., and Sha'bani, A.A., " *PSO-optimized modular neural network trained by OWO-HWO algorithm for fault location in analog circuits*", Neural Computing and Applications, April 2012, DOI 10.1007/s00521-012-0947-9, Print ISSN 0941-0643, Online ISSN 1433-3058, Publisher Springer-Verlag,

		10. In the paper: Jing Yuan Tang, Jian Ming Chen, Cai Zhang, *'Nonlinear Analog Circuit Fault Diagnosis Based on MFDFA Method* ', Applied Mechanics and Materials (Volumes 263 - 266), December, 2012, pp. 108-113, DOI 10.4028 /www.scientific.net/AMM.263-266.108. 11. In the paper: Bilski, P., and Wojciechowski, J., "*Current research trends in diagnostics of analog systems*", 2012 Int. Conf. on Signals and Electronic Systems (ICSES), 18-21 Sept. 2012, pp. 1 - 11. 12. In the paper: Yunyan, H. Minfang, P., Chenglai, T., and Hu, T., "*Analog Circuit Fault Diagnosis Using Multi-wavelet Transform and SVM*", 2012 Third Int. Conf. on Digital Manufacturing and Automation (ICDMA), July 31 2012-Aug. 2 2012, pp. 214 - 217. 13. In the paper: Antara Ain, Subhankar Mukherjee, Pallab Dasgupta, Siddhartha Mukhopadhyay, "*Post-silicon debugging of PMU integration errors using behavioral models*", Integration, the VLSI J., Available online 13 April 2012. 14. In the paper: Xhie Chun, Song Guo-ming, Jiang Shu-yan, WANG Hou-jun, "*Adaptive genetic algorithm optimized WNN approach for analog circuits soft fault diagnosis*," Application research of computers, Vol. 29, No. 1, Jan. 2012, pp.75-79 15. In the paper: Tian Xi-yu, Wang You-ren, Cui Jiang, "*Analog fault diagnosis technology based on clonal selection and clustering*", Transducer and Microsytem tchnologies, Vol. 28, No. 4, 2009, pp. 43-46. 16. In the paper: Yongkui, Sun, and Chen Guanju, and Li Hui, "*Analog circuit fault diagnosis method using adaptive wavelet analysis and SVM*", Chinese J. of scientific instrument, Vol. 29, No.10, Oct. 2008, pp. 1-4 17. In the paper: Che Bin, Fan Xiaoya**,** "*Testability Design for SoC Based on IDDQ Scanning*", Computer Measurement & Control,Vol. 17, No. 8, 2009. 18. In the paper: Chetouani, Y., "*Model selection and fault detection approach based on Bayes decision theory: Application to changes detection problem in a distillation column*", Process Safety and Environmental Protection, Elsevier, Available online, 4 March 2013, http://www.sciencedirect.com/science/article/pii/S0957582013000116. 19. In the paper: Liu Xiaoting, Liu Qingtao, Qiao Lixia, Jin Zhuo, "*Research on Graded Layout of Highway Maintenance Sites*

Based on Set Covering Theory", J. of Wuhan University of Technology (Transportation Science & Engineering), Vol. 37, No. 3, 2013.

20. In the paper: Lan Jingchuan, Huang Jianguo, "*The Application of Fault Dictionary in Analog Fault Recognition and Positioning*", Advances in information Sciences and Service Sciences(AISS) Volume4, Number10, June 2012, pp. 8-16.
21. Kumar, A., and Singh, A.P., "*Neural Network based Fault Diagnosis in Analog Electronic Circuit using Polynomial Curve Fitting*", Int. J. of Computer Applications (0975 – 8887) Vol. 61, No.16, Jan. 2013, pp. 28-34.
22. Jahangiri, M., Razaghian, F., "*Fault detection in analogue circuits using hybrid evolutionary algorithm and neural network*", Analog Integrated Circuits and Signal Processing, Springer, July 2014, http://dx.doi.org/10.1007/s10470-014-0352-7
23. Liu Xhiyuan and Peng Jiangxi, "*Analog circuit fault disgnosis based on EELM*", pp. 487-493, in "*Advanced Computer Control*", Jenny Ji, editor, WIT Press, Southampton SO40 7AA, UK.
24. Liang Wang, Wanggen Li, Lei Gao, "*A Novel Method for Logistics Facility Location by Combining Finite State Automaton and Genetic Algorithm*", International Conference on Artificial Intelligence and Industrial Engineering (AIIE 2015), Published by Atlantis Press.
25. Luo, H., Lu,W., Wang, Y., Wang, L., Zhao, X.,"*A novel approach for analog fault diagnosis based on stochastic signal analysis and improved GHMM*", Measurement, Volume 81, March 2016, Pages 26–35. doi:10.1016/j.measurement.2015.11.041.
26. Xin Gao, "*A novel method to optimum test-nodes selection in analog-circuit fault diagnosis*", 2014 Fifth IEEE Int. Conf. on Intelligent Control and Information Processing (ICICIP), Aug. 2014, Dalian, pp. 424 – 429, DOI: 10.1109/ICICIP.2014.7010291.
27. The thesis: A Kavithamani, A., "*Certain new approaches to fault diagnosis of analog electronic circuits using frequency response methods*" Anna University, Faculty of Electrical and Electronics Engineering, 2014, URI: http://hdl.handle.net/10603/24732.
28. In the paper: Zhou Jiangman, Huang Qingxiu, Peng Minfang,

		Yang Chao, Dong Na, "*Analog circuit fault diagnosis based on differential evolution and extreme learning machine.*" Computer Engineering and Applications, 2014, Vol. 50, No. 8, pp. 221-225. 29. In the paper: Tang, X, and Xu, A., **"***Practical Analog Circuit Diagnosis Based on Fault Features with Minimum Ambiguities*", Journal of Electronic Testing, February 2016, Vol. 32, No. 1, pp 83-95 First online: 14 Jan. 2016. 30. In the paper: Yanhong, H., and Jiali, W., "*Research on infrared diagnosis of circuit based on data fusion*", 12th IEEE International Conference on Electronic Measurement & Instruments (ICEMI), 2015, 10.1109/ICEMI.2015.7494193, pp. 53-57. 31. In the paper: Wang, L., Li, W., and Gao, L., "*A Novel Method for Logistics Facility Location by Combining Finite State Automaton and Genetic Algorithm*", Int. Conf. on Artificial Intelligence and Industrial Engineering (AIIE 2015), 2015. Published by Atlantis Press, pp. 365-368. 32. In the paper: Guoming, S., Qi, L., Gang, L., Shuyan, J., and Houjun, W., "*Analog circuit fault diagnosis using wavelet feature optimization approach*", 12th IEEE Int. Conf. on Electronic Measurement & Instruments (ICEMI), 2015, 10.1109/ICEMI.2015.7494225, pp. 119-124. 33. M Tadeusiewicz, S Hałgas, "*Diagnosis of a soft short and local variations of parameters occurring simultaneously in analog CMOS circuits*", Microelectronics Reliability, Vol. 72, May 2017, pp. 90-97. 34. Zhang, D., Feng, Z., "*Application of variational mode decomposition based demodulation Analysis in gearbox fault diagnosis*", IEEE Int. Instrumentation and Measurement Technology Conf. Proc. (I2MTC), May 2016, DOI: 10.1109/I2MTC.2016.7520586, Taipei, Taiwan. 35. Xiaofeng Tang ; Aiqiang Xu ; Ruifeng Li ; Min Zhu ; Jinling Dai, "Simulation-Based Diagnostic Model for Automatic Testability Analysis of Analog Circuits", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 37, No. 7, July 2018, pp. 1483 – 1493, DOI: 10.1109/ TCAD.2017.2762647.
xxx	**2**	The paper: (**5.c.52**) Litovski, V., Savić, M., and Mrčarica, Ž., "*Ideal Switch Model Cuts Significantly Simulation Time*", IEEE Circuits

		and Devices Magazine, ISSN: 8755-3996, Vol. 22, No. 4, July/August 2006, pp. 16-22, is cited 1. In the paper: Yildiz, A.B., "*A MNA-Based Unified Ideal Switch Model for Analysis of Switching Circuits*", J. of Circuits, Systems and Computers Volume 22, Issue 06, July 2013, Article Number: 1350046 2. Yildiz, A. B., "*Determination of unified time constants of switching circuits in terms of averaged-nodal equations*", Automatika Journal for Control, Measurement, Electronics, Computing and Communications, Print ISSN: 0005-1144 Online ISSN: 1848-3380, Vol. 58 , Iss. 1, 2017.
xxxi	**1**	The paper: (**5.c.54**) Anđelković, B., Litovski, **V.,** and Zerbe, V., "*Mission Level Modeling And Simulation Language For Mixed-Signal System-On-A-Chip Design*", J. of Circuits, Systems and Computers (World Scientific Publishing Company), Vol. 16, No. 1, February 2007, pp. 15-28. 1. was cited within the web page: http://www.mirrorservice.org/sites/home.ubalt.edu/ntsbarsh/Business-stat/RefSim.htm, entitled: Modeling & Simulation Resources. The subtitle in which the paper was cited was named: Journal Articles.
xxxii	**1**	The paper: (**5.c.57**) Sokolović, M., Litovski, V., Zwolinski, M., "*New Concepts of Worst Case Delay and Yield Estimation in Asynchronous VLSI Circuits***",** Microelectronics Reliability, ISSN 0026-2714, February 2009, Vol. 49, No. 2, pp. 186-198, is cited in: 1. The paper: Traver, V.J. and Bernardino, A. "*A review of log-polar imaging for visual perception in robotics*". In Proc. of Robotics and Autonomous Systems, Vol. 58, 2010, 378-398. http://marmota.dlsi.uji.es/WebBIB/papers/2010/Traver-RAS2010.pdf
xxxiii	**2**	The paper: (**5.c.58**) V. Litovski, and P. Petković, "*Why the Grid Needs Cryptography," Electronics*, Vol. 13, No. 1, June 2009, pp. 30-36, was cited: 1. In the paper: Bojković, Z., and Bakmaz, B., "*Smart Grid Communications Architecture: A Survey and Challenges*", In: Recent Researches in Applied Computers and Computational Science, Proceedings of the 11th WSEAS Int. Conf. on Applied Computer and Applied Computational Science (ACACOS '12), pp. 83-87. http://www.wseas.us/elibrary/conferences/2012/Rovaniemi/ACACOS/ACACOS-12.pdf 2. Soubhik Sarkar, "*Cognitive Radio Network for the Smart Grid*", Depart of Electronics, Carleton University.

		https://www.academia.edu/23010718/Cognitive_Radio_Network_for_the_Smart_Grid
xxxiv	**6**	The paper: (**5.c.62**) Andjelković, B., Litovski, V., and Zerbe, V., "*Grid-enabled Parallel Simulation Based on Parallel Equation Formulation*", ETRI J. (ISSN 1225-6463), Vol. 32, No. 4, August 2010, pp. 555-565, was cited: 1. In the paper: M. Zgurovsky, A. Petrenko, V. Ladogubets, O. Finogenov, B. Bulakh, "*WebALLTED: Interdisciplinary Simulator Based on Grid Services*", Proc. of the IEEE EWDTS, Kharkov, Ukraine, Sept. 2012, pp. 126-129. 2. In the paper: M. Zgurovsky, A. Petrenko, V. Ladogubets, O. Finogenov, B. Bulakh,"*WebALLTED: Interdisciplinary Modeling In Grid And Cloud*", Computer Science • 14 (2) 2013, pp. 295-306. 3. Latorre, J.-I., and Jiménez, E., "*Simulation-based optimization of discrete event systems with alternative structural configurations using distributed computation and the Petri net paradigm*", SIMULATION, November 2013, vol. 89 no. 11 pp. 1310-1334. 4. Limmer,S., Schneider,A., Boehme,C., Fey, D., Schmitz,S., Graupner, A., & Sülzle,M., "*Services for numerical simulations and optimisations in grids*", Int. J. of Parallel, Emergent and Distributed Systems, DOI: 0.1080/17445760.2013.842567, Published online: 24 Oct 2013. 6. Petrenko, A., Lobur, M., Ladogubets, V., Finogenov, O., Bulakh, B., Ladogubets, T., "*Simulation in GridALLTED Complex. The Experience of Designing and Application ofCAD Systems in Microelectronics*", 12-th Intern. Conf. "CADSM'2013", Feb. 2013, Polyana-Svalyava (Zakarpattya), Ukraine. Lviv: Publishing House Vezha Co, pp. 422–424.
xxxv	**1**	The paper: (**5.c.64**) Đorđević, S., Petković, P., and Litovski, V., „*A new topology oriented method for symbolic analysis of electronic circuits*", J. of Circuits, Systems, and Computers, Vol. 19, No. 8, 2010, pp. 1-15, was cited in: 1. Rahimi, M., Soleymani, B., Aminifar, F., Gholami, A., "A New Methodology for Circuit Analysis with Reverse Analysis Capability", J Circuit Syst. Comp. 26, 1750101 (2017) [24 pages]
xxxvi	**2**	The paper: (**5.c.66**) Andrejević Stošović, M., and Litovski, V., „*Hierarchical approach to diagnosis of mixed-mode circuits using Artificial Neural Networks*", Neural Network World, ISSN 1210-

		0552, Vol. 21, No. 2, 2011, pp. 153-168, was cited: 1. In the MSc thesis: Zhu, F., „Reconfigurable platform for prognostic design and evaluation“, Division of Research and Advanced Studies, University of Cincinnati, Department of Mechanical Engineering of the College of Engineering, 2011. 2. In the paper: Mansour Sheikhan, and Amir Ali Sha'bani, "*PSO-optimized modular neural network trained by OWO-HWO algorithm for fault location in analog circuits*", Neural Comput. & Applic., Springer-Verlag London Limited 2012, Published online 25.04.2012, http://www.springerlink.com/content/r4889w5242516707/fulltext.pdf It is written: **"As examples of ensemble/modular ANN-based fault diagnosis systems, Stosovic´ and Litovski [40] have applied ANNs to the diagnosis of mixed-mode electronic circuits. In order to tackle the circuit complexity and to reduce the number of test points, hierarchical approach to the diagnosis generation was implemented with two levels of decision: the system level and the circuit level. For each level, using the SBT approach, fault dictionary was created first. ANNs were used to model the fault dictionaries. At the topmost level, the fault dictionary was split into parts simplifying the implementation of the concept. A voting system was created at the topmost level in order to distinguish which ANN's output should be accepted as the final diagnostic statement."**
xxxvii	**2**	The paper: (**5.c.67**) Milojković, J. and V. Litovski, "*Short-term forecasting in electronics*", Int. J. of Electronics, ISSN: 0020-7217, Vol. 98, No. 2, 2011, pp. 161-172, was cited: 1. In the paper: Koffka Khan and Ashok Sahai, "*A Levy-flight Neuro-biosonar Algorithm for Improving the Design of eCommerce Systems*". J. of Artificial Intelligence, 2011,Vol. 4, pp. 220-232. 2. In the book: Maxwell, R. and Miller, T., "*Greening the media*", Oxford University Press, Oxford, 2012.
xxxviii	**9**	The paper: (**5.c.69**) Dimitrijević, M., and Litovski, V., „*Power Factor and Distortion Measuring for Small Loads Using USB Acquisition Module*", J. of Circuits, Systems, and Computers, Vol. 20, No. 5, August 2011, pp. 867-880, was cited: 1. In the paper: Liu, C. Y., Huang, C. F., and Huang, Y. C., *"Electric Power Usage Data Acquisition Module Composed of Two Sensors and a Microcontroller*", Proc. of the 2nd Int.

		Conf. of Intelligent Technologies and Engineering Systems, (ICITES2013), Lecture notes in Electrical Engineering 293, Springer, Switzerland 2014. 2. In the paper: Liu, C. Y., "*Smart Electric Receptacle with APP Accessibility*", http://ir.csu.edu.tw/bitstream/987654321/3088/2/CS-2-103-24-%E8%B3%87%E5%B7%A5%E7%B3%BB+%E5%8A%89%E5%BB%BA%E6%BA%90.pdf. 3. In the PhD thesis: Jacob, J., "*Comparing Security Concerns in the Adoption of Public Cloud Computing Based on Region of Residence*", Nortcentral Universisty, Prescott Valley, Arizona, USA, Dec 2016. 4. Yaseen, A.A., "*Fast-response power factor computation technique*", 2nd Int. Conf. on Advances in Computational Tools for Engineering Applications (ACTEA), Dec. 2012, DOI: 10.1109/ICTEA.2012.6462873, Beirut, Lebanon. 5. Gligor, A., Muntean, R., and Dumitru, C-D., "*Digital Solution for Fast Evaluation of the Power Factor in Power Networks*", Scientific Bulletin of the "Petru Maior" University of Targu Mures, Tirgu Mures, Vol. 14, Iss. 1, 2017, pp. 12-16. 6. Králiková, E., Čičáková, O., "*Distortion Power Measurements in Education*", Measurement 2013, Proc. of the 9th Int. Conf., Smolenice, Slovakia, pp. 75-78. 7. Gligor, A., Dumitru, C.D., Ronay, K., and Muntean, R., "*Microcontroller Based Prototype for Reactive Power Compensation in Local Distribution Networks*", Procedia Engineering, Vol. 181, 2017, pp. 746-753, open access. 8. Liu J., "*Integration of smart electronics and embedded system teaching internship research and development*", [Information Engineering] research report, 2013, http://ir.csu.edu.tw/handle/987654321/3028 9. Liu, J., "*Smart Electric Receptacle with APP Accessibility*", [Information Engineering] research report, Project Number: CS-2-103-24, 2016. http://ir.csu.edu.tw/handle/987654321/3088.
xxxix	**5**	The paper: (**5.c.72**) Andrejević Stošović, M., Milić, M., Zwolinski, M., Litovski, V.,"*Oscillation-based analog diagnosis using artificial neural networks based inference mechanism*", COMPELECENG-D-11-00818R3, Computers and Electrical Engineering, Vol. 39, 2013, pp. 190-201. ISSN: 0045-7906, Impact Factor: 0.928, was cited 1. In the apaper: Khoukhi, A., and Khalid, M.H., "*Hybrid computing techniques for fault detection and isolation, a review*", Computers & Electrical Engineering, Volume 43,

		April 2015, pp. 17–32. 2. In the apaper: Mosin, S., "*An Approach to Design-for-Testability Automation of Analogue Integrated Circuits Using OBIST Strategy*", 5th Mediterranean Conf. on Embedded Computing, MECO 2016, Bar, Montenegro, pp. 211-214. 3. In the apaper: Senani, R., Bhaskar, D.R., Singh, V.K., and Sharma, R.K."*Sinusoidal oscillators and waveform generators using modern electronic circuit building blocks*", Springer, 2016. 4. In the apaper: M Hasan, Y Zhu, Y Sun, "Oscillation-Based DFT for Second-Order Bandpass OTA-C Filters", Circuits, Systems, and Signal Processing", pp 1–18 , Springer, 2017. https://link.springer.com/article/10.1007/s00034-017-0648-9 5. In the apaper: D Binu, BS Kariyappa, "A survey on fault diagnosis of analog circuits: Taxonomy and state of the art", AEU - International Journal of Electronics and Communications, Vol. 73, March 2017, pp. 68-83.
xL	**2**	The paper: (**5.c.76**) Dimitrijević, M., Andrejević Stošović, M., Milojković, J., Litovski, V., "*Implementation Of Artificial Neural Networks Based AI Concepts to the Smart Grid*", Facta Universitatis, Series: Electronics and Energetics Vol. 27, No 3, September 2014, pp. 411 - 424. DOI: 10.2298/FUEE 1403411D, was cited 1. In the apaper: Janjic, A., Savic, S., Janackovic, G., Stankovic, M., and Velimirovic, L., "Multi-Criteria Assessment of the Smart Grid Efficiency Using the Fuzzy Analytic Hierarchy Process", Facta Universitatis, Series: Electronics and Energetics Vol. 29, No 4, December 2016, pp. 631 - 646 DOI: 10.2298/FUEE1604631J 2. In the apaper: Siddavaatam, P., Sedaghat, R.,"A Novel Architecture with Scalable Security Having Expandable Computational Complexity for Stream Ciphers" Facta Universitatis, Series: Electronics and Energetics Vol. 30, No 4, December 2017, pp. 459 - 475 DOI: 10.2298/FUEE1704459S
xLi	**1**	The paper: (**5.c.77**) Andrejević Stošović, M., Litovski, I., Lukač, D., Dimitrijević, M., and Litovski, V., "*Small Signal Model of a Solar Cell"*, Simulation, Trans. of the Society for Modeling and Simulation, International. Published online 1 October 2014, Oct. 01, 2014, Impact factor=0.692, was cited 1. In the apaper: ", Badoud, A. E. Raison, B., Vila, L. L. F., Bouamama, B. O., and Khemliche,M., "Modeling, simulation

		and hardware implementation of a bond graph-maximum power point tracker for a photovoltaic panel under partially shaded conditions", Simulation, Trans. of the Society for Modeling and Simulation, International. Published online before print June 24, 2016, DOI: 10.1177/0037549716646846
xLii	**1**	The paper: (**5.c 82**) Milić, M., and Litovski, V., "*Oscillation-based testing method for detecting Switch faults in high-q sc biquad filters*", Facta Universitatis, Series: Electronics and Energetics, Vol. 28, No 2, June 2015, pp. 223 - 236 DOI: 10.2298/FUEE1502223M, is cited in: 1. Masood-ul Hasan, Yanqing Zhu, Yichuang Sun, "Oscillation-Based DFT for Second-Order Bandpass OTA-C Filters", Circuits, Systems, and Signal Processing, ISSN: 0278-081X (Print) 1531-5878 (Online), First Online: 06 September 2017, pp. 11-18.
xLiii	**1**	The paper: (**5.c.86**) Andrejević Stošović, M., Dimitrijević, M., Bojanić, S., Nieto-Taladriz, O., **Litovski, V.,** "Characterization of Nonlinear Loads in Power Distribution Grid", Facta Universitatis, Series Electronics and Energetics, Vol. 29, No. 2, 2016, pp. 159-175, was cited 1. In the paper: Vujnović, S., Marjanović, A., Đurović, Ž., Tadić, P., Kvaščev, G., "Toward Acoustic Noise Type Detection Based on QQ Plot Statistics" , Facta Universitatis, Series: Electronics and Energetics Vol. 30, N o 4 , December 2017, pp. 571 - 5 84 DOI: 10.2298/FUEE170 4571V.
xLiv	**1**	The paper: (**5.d.21**) Zarković, K., Ranđelović, Z., Milenković, S., Novaković, M., Jovanović, Lj., **Litovski, V.,** *"JUDGE - Jacquard Developing Environment (Editor)"*, Tekstilna industrija, 3-4/97, Beograd, 1997, was cited: 1. In the overview of the textile design software, at a Vietnameses site: (*www.cesti.gov.vn/webcms/jsp/download/maydetjacquard.htm*), five packages are mentioned among which (JUD-GE) developed in LEDA under the leadership of Prof. Litovski. The package was described in the above reference.
xLv	**2**	The paper: (**5.d.29**) B. Jovanović, M. Damnjanović, V. Litovski, „*Square Root on Chip*", ETF J. of Electrical Engineering, A Publication of the EE Department, University of Montenegro, May 2004, Vol.12, No.1, YU ISSN: 0353-5207, was cited 1. In the project task: Reddy, S. and Srivastava, U., "*Area optimized square root and dividet unit for multimedia*

		processing application", George Mason University, Fairfax, Virginia, Dept. Electrical and Computer Engineering, http://ece.gmu.edu/courses/ECE645/projects_S05/specs/SQR_DIV_shilpa_utkarsh.pdf 2. In the paper: Naji, H.R., "*Solving Complex Computational Problems Using Multiagents Implemented in Hardware*," Computing in Science and Engineering, Vol. 10, No. 5, pp. 54-63, Sep./Oct. 2008, doi:10.1109/ MCSE.2008.121.
xLvi	**5**	The paper: (**5.e.7**) Pantić, D., Milenković, S., Trajković, T., Litovski, V., Stojadinović, N., *"Inverse Modeling of Semiconductor Manufacturing Processes"*, 20th Int. Conf. on Microelectronics MIEL '95, Vol. 1, Niš, 12-14 Sep., 1995, pp. 321-326, is cited: 1. In the paper: L. Capodieci, R. Subramanian, B. Rangarajan , W. D. Heavlin, J. Li, D. A. Bernard, and V. V. Boksha, " *Novel methodology for postexposure bake calibration and optimization based on electrical linewidth measurement and process metamodeling*", J. of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Nov. 1998 , Vol. 16, No. 6, pp. 3752-3758, 2. The MSc thesis: Chiang, M.-L., "*Process Recipe Optimization in Multiple Response System*", Chung Yuan Christian University, Department of Mechanical engineering, 2001 (URN: etd-0813102-120054), as well as in 3. In the paper: Flax, M.R. and Jin, J.S. "*A matrix approach to neural network inversion*", Proc. of the ICONIP '99. 6th Int. Conf. on Neural Information Processing, 1999, Vol. 1, Perth, WA, Australia, pp. 85-90. 4. In the paper: Vural, R.A., Kahraman, N., Erkmen, B., and Yildirim T., "*Process Independent Automated Sizing Methodology for Current Steering DAC*", Int. J. of Electronics, Published online: 03 Jan 2015, DOI: 10.1080/00207217.2014.989924. 5. Kahraman, N., Erkmen, B., Yildirim, T., "*Threshold Voltage Modeling Using Neural Networks*" Neural Network World: Int. J. on Neural and Mass - Parallel Computing and Information Systems; Prague Vol. 19, Iss. 3, (2009), pp. 255-262.
xLvii	**1**	The paper: (**5.e.8**) Litovski, V., Ranđelović, Z., Damnjanović, M., *"Routing In Standard Cells"*, 20th Int. Conf. on Microelectronics, MIEL '95, Vol. 2, Niš, Sep. 1995, pp. 461-466, was cited: 1. In the paper: Mªde las Mercedes Gómez-Albarrán, Ana Mª

		Fernández-Pampillón-Cesteros and Juan Manuel Sánchez-Pérez , "*A routing strategy based on genetic algorithms*", Microelectronics Journal, Vol. 28, No. 6-7, August-September 1997, pp. 641-656.
xLviii	**1**	The paper: (**5.e.10**) Litovski, V.B., and Andrejevic, M., "*Electronic modelling using ANNs for analogue and mixed-mode behavioural simulation*", Invited paper, In: 6th Seminar on neural network applications in electrical engineering, NEUREL '02; 26–28 September 2002. p. 113–8, was cited: 1. In the paper: Mohammadi, K., and Mahdavi, S.J.S, "*On improving training time of neural networks in mixed signal circuit fault diagnosis applications*", Microelectronics and Reliability, Vol. 48, No. 5, 2008, pp. 781-793.
iL	**2**	The paper: (**5.g.5**) Litovski, V., Petković, P., *"Time Domain Temperature Dependence Simulation Of MOS Electronic Circuits"*, Proc. of the 6th Int. Conf. on computers in design engineering, CAD84, Brighton, April, 1984, pp. 61-66, was cited: 1. Živić**,** Z., Živić, A., and Stojadinović, N., "*A new CMOS IC structure and its characterization* ", Microelectronics Reliability, Vol. 25, No. 1, 1985, pp. 123-146, the following is cited 2. In the paper: Dokić, B.L., Ilisković, A.J., and Bundalo, Z.V., **"***CMOS gates with regenerative action at one of inputs***",** Microelectronics Journal, Vol. 19, Issue 3, May-June 1988, pp. 17-20.
L	**2**	The paper: (**5.g.33**) Mrčarica, Ž, Ilić, T., Glozić, D., Litovski, V., and Detter, H., "*Mechatronic Simulation Using Alecsis: Anatomy of the Simulator*", Proc. of the Eurosim'95, Vienna, Austria, Sept. 1995, pp. 651-656, was cited in 1. In the invited paper: Senturia, S. D., "*CAD challanges for Microsensors, Microactuators, and Microsystems*", invited paper, Proc. of the IEEE, Vol. 86, No. 8, August 1998., pp. 1611-1626. 2. Pelz, G., "*Mechatronic Systems"*, John Wiley & Sons, Ltd, 2003, Print ISBN: 0470849797, Online ISBN: 0470867906.
Li	**14**	The paper: (**5.g.35**) Panić, V., Milovanović, D., Petković, P., Litovski, V., *"Fault Location In Passive Analog RC Circuits By Measuring Impulse Response"*, 20th Int. Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 517-520, was cited: 1. In the paper: Sindia, S., Singh, V., and Agrawal, V.,"*Bounds on Defect Level and Fault Coverage in Linear Analog Circuit Testing*", 13th IEEE/ VSI VDAT2009, VLSI Design And Test Symposium, July 2009, Electonic City, Hosur Road, Bangalo-

		re, India, 2. In the paper: Sindia, S., Singh, V., and Agrawal, V.,*"Polynomial Coefficient Based DC Testing of Non-Linear Analog Circuit***s",** Proceedings of the 19th ACM Great Lakes symposium on VLSI**,** *GLSVLSI'09,* May 10–12, 2009, Boston, Massachusetts, USA, Pages 69-74 , SBN:978-1-60558-522-2. kao i u 3. In the paper: Sindia, S., Singh, V., and Agrawal, V., "*Multi-Tone Testing of Linear and Nonlinear Analog Circuits using Polynomial Coefficients*", IEEE Asian Test Symposium (ATS) 2009, Taichung, Taiwan, Nov 2009, pp. 63-68. 4. In the paper: Sindia, S., Singh, V., and Agrawal, V., "*V-Transform: An Enhanced Polynomial Coefficient Based DC Test for Non- Linear Analog Circuits*", 7th IEEE East-West Design & Test Symposium, EWDTS 2009, Moscow, Russia, September 18 -21, 2009, http://www.eng.auburn.edu/~vagrawal/TALKS/EWDTS09/ewdts09-31.pdf, 5. In the paper: Sindia, S., Singh, V., and Agrawal, V., "*Polynomial Coefficient Based Multi-Tone Testing of Analog Circuits*", Proc. of the 18th North Atlantic *Test Workshop*, pp. 6–15, May 2009. http://www.eng.auburn.edu/~vagrawal/TALKS/ATS09/nft_ieee.pdf 6. In the paper: Sindia, S., Singh, V., and Agrawal, V.," *Parametric Fault Diagnosis of Nonlinear Analog Circuits using Polynomial Coefficients*", 23rd Int. Conf. on VLSI Design, VLSID 2010, Bangalore, India, January 2010, pp.288-293. www.eng.auburn.edu/~vagrawal/TALKS/VD10/PID1061303.pdf. 7. In lecture notes: Lin, C.V., "*Fault Diagnosis of Analog Circuit*", MSIC D&T Lab., Dept. of Electrical Eng., National Yunlin University of Science and Technology, NYUST, Taiwan, http://140.125.35.23/course/Special_topic_in_testability_of_Analog_and_Mixed_Signal_VLSI_circuit/CH5_fault_diagnosis.pdf 8. Sindia, S., Agrawal, V.D., and Singh, V., "*Distinguishing Process Variation Induced Faults from Manufacturing Defects in Analog Circuits using V-Transform Coefficients*", ww.eng.auburn.edu/~agrawvd/TALKS/SSST11/vt_dc_ieee.pdf 9. In the paper: Sindia,S., and D. Agrawal, V.D., "*Non-Linear Analog Circuit Test and Diagnosis under Process Variation using V-Transform Coefficients*", Proceedings of the 29th IEEE VLSI Test Symposium, Dana Point, Ca, USA, 2011, pp. 64-69.

		10. In the paper: P. Boi and A. Montisci, "*A Neural Based Approach and Probability Density Approximation for Fault Detection and Isolation in Nonlinear Systems*", IFIP Advances in Information and Communication Technology, 2011, Vol. 363/2011, pp. 296-305, DOI: 10.1007/978-3-642-23957-1_34. 11. In the paper: Sindia, S., Agrawal, W. D., and Singh, V., "*Defect Level and Fault Coverage in Coefficient Based Analog Circuit Testing*", J. of Electronic Testing, 2012, DOI: 10.1007/s10836-012-5305-4. 12. In the Proposal for PhD thesis: Sindia, S., "High Sensitivity Test Signatures for Unconventional Analog Circuit Test Paradigms", A Proposal for Ph.D. Dissertation Dept. of ECE, Auburn University, AL, USA, March 22, 2012. 13. In the paper: Sindia, S., Agrawal, V.D., Singh, V., "*Parametric Fault Testing of Non-Linear Analog Circuits Based on Polynomial and V-Transform Coefficients*", Electron Test, 2012, Vol. 28, pp. 757–771, DOI 10.1007/s10836-012-5326-z. 14. In the PhD thesis: Sindia, S., "*High Sensitivity Signatures for Test and Diagnosis of Analog, Mixed-Signal and Radio-Frequency Circuits*", Submitted to the Graduate Faculty of Auburn University, Auburn, Alabama, August 3, 2013
Lii	**2**	The paper: (**5.g.36**) Damnjanović, M., Dimić, Ž., Litovski, V., and Glozić, D., "*Hardware description language for Alecsis simulator*", Proc. of the 20th Conf. on Microelectronics, 1995, Vol. 2, pp. 525-528, was cited in: 1. Endemano, A., Fourniols J. Y., Camon H., Marchese A., Muratet S., Bony F., Dunnigan M., Desmulliez M. P. Y., and Overton G. **(Mentor Graphics (UK) Ltd,** Rivergate, Newbury Business Park, London Road, Newbury, Berkshire RG14 2QB, UK) "*VHDL-AMS modelling and simulation of a planar electrostatic micromotor*", J. of Micromechanics and Microengineering, Vol. 13, 2003, pp. 580-590. It is written: "**Their use, however, requires a substantial understanding of the underlying physical behavior** and ... [4-6]. As [5] the above was cited. 2. In the US patent: Meyer, S. J., "*Mixed signal simulation*", Application Number: EP20010954620, Patent EP1305765, Publication Date: 05/02/2003.
Liii	**7**	The paper: (**5.g.38**) Mrčarica, Ž., Glozić, D., Litovski, V., Detter, H.,

		"Simulation Of Microsystems Using A Behavioural Hybrid Simulator Alecsis", u: Adey, R.A., Lahrmann, A., Lemboe Ilmann, C., editors, "*Simulation and Design of Microsystems and Microstructures*", Computational Mechanics Publication, Transactions on the Built Environment, Vol. 12, © 1995 WIT Press, www.witpress.com, ISSN 1743-3509, Southampton, GB, 1995, was cited 1. In the paper: Gerlach, G., Schroth, A., und Klein, A., "*Modellirung nichtelektrischer Komponenten in heterogenen und komplexen Mikrosystemen*", Workshop: Methoden und Werkzeuge zum Entwurf von Microsystemen, Frankfut a.M., Juni 1996, pp. 12-21, is written: **"Die partielle DGL wird ein System gewoenlicher DGL ueberfuert (z.B. durch einen Finite-Differenzen-Ansatz) und direct als Syntax in den Systemsimulator eingegeben [14].** The cited reference is as above. 2. In the paper: Klein, A., and Gerlach, G., "*Modeling of piezoelectric bimorph structures using an analog hardware description language*", ibid. pp. 229-238. 3. In the paper: Bielefeld, J., Pelz, G., and Zimmer, G., "*Electrical network formulation of mechanical finite-element models*", ibid. pp. 239-247. 4. In the paper: Bielefeld, J., Pelz, G., and Zimmer, G., ¨*AHDL-model of a 2D mechanical finite-element usable for micro-electro-mechanical-systems*¨, Proc. of the IEEE/VIUF workshop on behavioral modeling and simulation, 1977, pp. 177-181. 5. In the paper: Petrenko, A.I., "Networked VLSI and MEMS designer for Grid", Proc. of the Design & Test Symposium (EWDTS), 2010 East-West, St. Petersburg, Sept. 2010, pp. 538 – 544. 6. In the PhD thesis: Voßkämper, L. M.,, "Kohärente Layoutsynthese und Modellbildung von skalierbaren mikroelektromechanischen Strukturen", submitted at 24. January 2003, at the Gerhard-Mercator-Universität, Duisburg, Germany, deposit.ddb.de/cgi-bin/dokserv?idn=96653767x&dok_var=d1&dok_ext=pdf&filename=96653767x.pdf, 7. In the book: Pelz, G., *"Mechatronic Systems"*, John Wiley & Sons, Ltd, 2003, Print ISBN: 0470849797 , Online ISBN: 0470867906.
Liv	**9**	The paper: (**5.g.39**) Milenković, S., Obradović, Z., and Litovski, V., "*Annealing Based Dynamic Learning in Second-Order Neural Networks*", Int. Conf. on Neural Networks, ICNN '96, Washington, D.C., USA, 3.-6. June 1996, pp. 458-463, was cited:

		1. In the paper: Engelbrecht, A.P. and Ismail, A., "*Training Product Unit Neural Networks",* Stability and Control: Theory and Applications, Vol. 2, No 1-2, pp 59-74, 1999, ISSN 1563-3276, **One claims that second order synapses in artificial neural networks were introduced for the first time** in the above reference. 2. In the paper: A. Ismail A. and Engelbrecht, A. "*Training Product Units in Feedforward Neural Networks using Particle Swarm Optimization*". In Proc. of the Int. Conf. on Articial Intelligence, Durban, South Africa, pages 36-40, 1999 and in 3. In the paper: Ismail, A., and Engelbrecht, A.P., "*Global optimization algorithms for training product unit neural networks*", IEEE-INNS-ENNS Int. Joint Conf. on Neural Networks, IJCNN`00. Vol. 1, Como, Italy, July 24-July 27, ISBN: 0-7695-0619-4, pp. 1132. 4. In the paper: de Nicolas-Presa, Jaime M., de la Mata-Moya, D., Jarabo-Amores, M.-P., Barcena-Humanes, J.-L., and Palma-Vazquez, A., "*High-order neural network-based ship detection algorithms applied to SAR imagery* ", EUSAR. 9th European Conf. on Synthetic Aperture Radar, 2012**,** Nuremberg, Germany, April 2012, pp. 555 – 558 5. *In the Master Thesis: Επιτροπάκης, M., "*Εκπαίδευση τεχνητών νευρωνικών δικτύων με την χρήση εξελικτικών αλγορίθμων, σε σειριακά και κατανεμημένα συστήματα*", Πανεπιστήμιο Πατρών, Σχολή Θετικών Επιστημών, Τμήμα Μαθηματικών, Πάτρα 2008. http://nemertes.lis.upatras.gr/jspui/handle/10889/1245. 6. In the papar: Epitropakis, M.G. , Plagianakos, V.P., and Vrahatis, M.N., "*Evolutionary algorithm training of higher order neural networks*", Chapter in: Zhang, M., "*Artificial higher order Neural networks for computer science and engineering, Trends for emerging applications*", Information Science Reference, Hershey, NY, USA, 2010. 7. In the PhD: Shah, S., "*Musculoskeletal simulation of upper extremity motion: Effect of selective muscle weakness and application to rehabilitation*", University of Delaware, ProQuest Dissertations Publishing, 2009. 8. In the papar: Hernández, G., Zamora, E, and Sossa, H., "*Comparing Deep and Dendrite Neural Networks: A Case Study*", Mexican Conference on Pattern Recognition, MCPR 2017: Pattern Recognition pp 32-41 , Part of the Lecture Notes in Computer Science book series (LNCS, volume 10267).

		9. *In the papar: Επιτροπάκης, M., "*Ανάπτυξη και θεμελίωση νέων μεθόδων υπολογιστικής νοημοσύνης, ευφυούς βελτιστοποίησης και εφαρμογές*", 2014-07-17, Appears in Collections: Πανεπιστήμιο Πατρών, Τμήμα Μαθηματικών (ΔΔ). http://hdl.handle.net/10889/7885
Lv	**2**	The paper: (**5.g.40**) Marković, V., Petković, P., Litovski, V., *"Symbolic Approach To The Microwave Circuit Design"*, XI Int. Microwave Conf. MICON '96, Warsaw, 27-30 May, 1996, was cited: 1. In the paper: Damiano, J.-P. Scotto, M. Ribero, J.-M., "*Computer-algebra systems and electromagnetic problems*", IEEE Antennas and Propagation Magazine, Publication Date: Dec 1996, Volume: 38, Issue: 6, On page(s): 92-98, ISSN: 1045-9243, 2. In the paper: Damiano, J.-P. and Ghio, G. , "*Computer algebra systems applied to some electromagnetic problems*", Annales des Telecommunications/Annals of Telecommunications, Vol.52, No. 5-6, May 1997, pp. 306-318.
Lvi	**6**	The paper: (**5.g.45**) Mrčarica, Ž., Detter, H., Glozić, D., Litovski, V., *"Describing Space-Continous Models of Microelectromechanical Devices For Behavioural Simulation"*, European Design Automation Conf., EURO-DAC '96 with EURO-VHDL '96, Geneva, 16-20 Sep., 1996, pp. 316-321, is cited: 1. In the paper: Hofmann, K., Glesner, M., Sebe, N., Manolescu, A., Marco, M., Samitier, J., Karam, J.-M., Courtois, B., "*Generation of the HDL-A-model of a Micromembrane from its Finite-element-description*", ED& TC'97, Paris, France, pp.108--112, March, 1997 , and 2. In the paper: Karam, J.M., Courtois, B., Boutamine, H., Drake, P., Rencz, M., Poppe, A., Szkely, V., Hofmann, K., Glesner, M., "*CAD and foundries for microsystems*", Proc. of the 1997 Design Automation Conf., Anaheim, CA, June 1997, pp. 674-679, 3. In the chapter: Bungartz, H.-J., Frank, A., Meier, F., et al., "*Fluid Structure Interaction: 3D Numerical Simulation and Visualization of a Micropump*", TUM-19710, as a chapter in "*Methoden und Werkzeuge fuer die nutzukg paralleler Architekturen*", published by: Fakultaet fuer Informatik der TechnischenUniversitaet Muenchen, 1997, 4. In the curriculum: Bungartz, H.-J., Frank.A, and Meier, F., "*Design and Implementation of a Modular Environment for*

		Coupled Systems", within: "*Matematische modelirung , simulation und verification in materialorientierten Prozessen und intelligenten systemen*", Sonderforschungsbereich 438, Technische Universitaet Muenchen, Universitaet Augsburg, April 1998. 5. In the Ph.D. Thesis: Ramaswamy, D., "*Simulation Tools for Micro-ElectroMechanical System*", Ph.D. Thesis, MIT, Boston, MA, May 2001. 6. In the Mastre thesis: Abd Rahman, A. B., "*Modelling of mixed physical-domain system*", University of Southampton, School of Electronics and Computer Science, Masters Thesis, 2010, 133pp.
Lvii	**5**	The paper: (**5.g.46**) Mrčarica, Ž., Litovski, V. B., Delić, N. and Detter, H., "*Modelling of micromechanical devices using hardware description language*", Int. Conf. on Micro System Technologies, 1996, pp. 293–298, was cited: 1. Gerlach, G. and Klein, A., "*Strategies of modelling and simulation of microsystems with electromechanical energy conversion*", Microelectronics Journal**,** Volume 29, Issue 11, Nov. 1998, Pages 773-783. 2. In the book: Pelz, G., "*Mechatronic Systems"*, John Wiley & Sons, Ltd, 2003, Print ISBN: 0470849797, Online ISBN: 0470867906. 3. In the PhD thesis: Voßkämper, L. M., "*Kohärente Layoutsynthese und Modellbildung von skalierbaren mikroelektromechanischen Strukturen*", submitted at 24. January 2003, at the Gerhard-Mercator-Universität, Duisburg, Germany, deposit.ddb.de/cgi-bin/dokserv?idn=96653767x&dok_var=d1&dok_ext=pdf&filename=96653767x.pdf, 4. In the PhD thesis: Luedecke, A., "*Simulationsgestuetzte Verfahren fuer den Top-Down Entwurf heterogener Systeme*", Universitaet Duisburg, Essen, Germany, December 2003. 5. In the Mastre thesis: Abd Rahman, A. B., "*Modelling of mixed physical-domain system*", University of Southampton, School of Electronics and Computer Science, Masters Thesis, 2010, 133pp.
Lviii	2	The paper: (**5.g.48**) Kero, N., Janković, S., Fallman, W., and Litovski, V., "*A High Speed Serial Bus Controller ASIC*", Proceedings of MIEL'97, Niš, Yugoslavia, 1997, pp. 737-742, was cited in 1. In the report for the project: The Technical University of Vienna, 1997 god., in the report for the project: "*UNICHIP Vienna - ASIC Design with Austrian Universities*",

		http://www.iaae.tuwien.ac.at/gme/jb97/ 97_59.htm. 2. In the paper: Sang-Woo Park, Yong-Hwan Lee, "*Serial Interface for mobile processors*", Korea Institute of Information Technology, Volume 7, No. 1, 2009.2, pp. 38-43.
Lix	**2**	The paper: (**5.g.49**) Janković, S., Maksimović, D., Petković, P., Litovski, V., *"Testable Design Of Digital ASIC With Embedded Analog Multiplexers"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 779-782, was cited: 1. In the paper: Rodriguez-Montanes, R., Balado, L., and Figueras, J., » *Quiscent defective behaviours of analog multiplexers*", Proc. of the XVII Conf. on design of circuits and integrated Systems, Santander, Spain, DCIS 2002, ISBN 84-8102-311-6, Nov. 2002, pp. 333-338, the following was cited 2. In the paper: Zhizong Ren, Yongxin Zhu, Zhijun Li, Tingting Mo, Xiaoyi Ding, and Jie Zhong, "*On Driving Micro Motors for MEMS with a Micro Driver Based on Three-Phase Sinusoidal Signals*", Fifth IEEE Int Symp. on Embedded Computing, SEC '08 , Oct. 2008, pp. 237 – 242, Beijing, China, ISBN: 978-0-7695-3348-3.
Lx	**2**	The paper: (**5.g.55**) Ž. Mrčarica, Z. Randjelović, M. Jakovljević, V. B. Litovski, H. Detter, "*Methods for description of microelectromechanical device models for system-level simulation*", MICROSIM II, Proc. of the Conf. On Simulation and Design of Microsystems and Microstructures MICROSIM '97, Lausanne, Switzerland, September 1997, pp. 271-280, was cited in: 1. Pelz, G., "*Mechatronic Systems"*, John Wiley & Sons, Ltd, 2003 , Print ISBN: 0470849797, Online ISBN: 0470867906. 2. In the PhD thesis: Voßkämper, L. M., "*Kohärente Layoutsynthese und Modellbildung von skalierbaren mikroelektromechanischen Strukturen*", submitted at 24. January 2003, at the Gerhard-Mercator-Universität, Duisburg, Germany. deposit.ddb.de/cgi-bin/dokserv?idn=96653767x& dok_var=d1&dok_ext=pdf&filename=96653767x.pdf.
Lxi	**2**	The paper: (**5.g.71**) Petković, P., Đorđević, S., **Litovski, V.**, "*A New Approach To Symbolic Analysis Of Large Circuits*", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 687-690, is cited in 1. In the paper: Feng, L., and Zhang, Y., "*Parallel topological analysis of circuits*", Information and Elecronic Engineering, Vol. 6, No. 3, June 2008. 2. In the paper: Stakhiv, P., and Cegielski, M., " Stability of parallel computations of transient processes in the electric

		circuits", Przegląd Elektrotechniczny, 2007-II.
Lxii	**1**	The paper: (**5.g.72**) Panić, V., Janković, S., Milovanović, D., Litovski, V., "*Cell Design for Boundary-Scan Implementation* ", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 719-722, was cited: 1. In the MSc thesis: Karlsson, M., "*Test system for improved hardware tests*", (A master of science thesis project done in cooperation with Mälardalens University and ABB robotics), http://www.idt.mdh.se/utbildning/exjobb/files/TR0552.pdf.
Lxiii	**3**	The paper: (**5.g.74**) Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., Litovski, V., "*Analogue Behavioural Simulator as a Tool for Coupled Electro-Thermal Analysis of Microsystems*", Proc. of the 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 561-564, was cited 1. In the paper: Sabry, M.-N., "*Dynamic Compact Thermal Models Used for Electronic Design: A Review of Recent Progress*" ASME Int. Electronic Packaging Technical Conf. and Exhibition, Volume 1, Maui, Hawaii, USA, 2003, Paper No. IPACK2003-35185, pp. 399-415. 2. Lasance, C., Sabry, M.N., and A Bar-Cohen, Chapter 7: "*Techniques to Create Compact Thermal Models—Dynamic Problems*" in *Encyclopedia of Thermal Packaging* Vol. 3: *Compact Thermal Models of Electronic Components*, World Scientific, 2014. 3. Lasance, C., Sabry, M.N., and A Bar-Cohen, Chapter 6: "Techniques to Create Compact Thermal Models—Steady State Problems", ibid.
Lxiv	**5**	The paper: (**5.g.83**) Andrejević, M., Milovanović, D., Petković, P., Litovski, V., "*Extraction of Frequency Characteristics of Switched-Capacitor Circuits Using Time-Domain Analysis*", Proc. of IEEE 23th Int. Conf. on Microelectronics (MIEL2002), Niš, 12.5.-15.5.2002, pp. 635-638, ISBN 0-7803-7235-2 was cited: 1. In the paper: Shen Haibin, Li Xiaoming, Yu Jun, Pan Xuezeng, and Yan Xiaolang, "*The Noise Model and Fast Simulation of A Random Number Generator*", J. of System Simulation, Vol. 16, No. 4, 2004, http://d.wanfangdata.com.cn/periodical_xtfzxb200404057.aspx 2. In the paper: Li Xiao-ming, Shen Hai-bin Yan Xiao-lan, "*Characteristic Analysis of a Chaotic Random Number Generator Using Piece-Wise-Linear Map*", J. of Electronics & Information Technology, Vol. 27, No. 6, Jun 2005.

		3. Jun, Y., Haibin, S., and Xiaolang, Y., "*Implementations of chaos-based high-speed truly random number generator*", Chinese J. of Semiconductors, Vol. 25, No. 8, 2004, pp. 1013-1018. 4. GAO Jin, Song Li, "Frequency Domain Analysis of Switching Capacitor Filter", https://translate.google.rs/translate?hl=en&sl=zh-CN&u=http://www.chinaaet.com/article/7961&prev=search 5. Wang Yunfeng , Shen Haibin , and Yan Xiaolang, "*Design of a Chaotic Random Number Generator*", Chinese J. of Semiconductors, Vol . 26, No . 12, Dec., 2005, pp. 2433.2439
Lxv	**4**	The paper: (**5.g.84**) Maksimović, D.M., Litovski, V.B., "*Timing Simulation with VHDL Simulators*", Proc. 23rd Int. Conf. on Microelectronics (MIEL 2002), Nis, Yugoslavia. 12-15 May, 2002, pp. 655-658, was cited: 1. In the paper: Minjie, M., Zheying, L., Guangyu, J., "*Study on analyzing and modeling of delay activity for digital circuit*", ASICON 2005, Proc. of the 6th Int. Conf. on ASIC, Volume 2, 2005, Article number 1611420, Pages 681-684**,** 2. In the Master thesis: Chou, G., "*The design of MIPS Central Process Unit (Using VHDL)*", http://thesis.lib.cycu.edu.tw/ETD-db/ETD-search-c/view_etd?URN=etd-0611106-122050. 3. In the paper: Zdraveski, Z., Dimitrovski, D., and Trajanov, D., "*HDL IP Cores System as an Online Testbench Provider*", Proc. of the Small Systems Simulation Symposium, SSSS' 2014, Niš, Serbia, 108-112. 4. Graziano, D., Hitchcock, J., Rilling, J., Meyer, T., and Wang, X.,"*A Case Study of Hardware Trojan Design and Implementation for the 2010 Embedded Systems Challenge*", http://isis.poly.edu/esc/2010/Reports/Iowa%20State%20University%20-%20David%20Graziano.pdf
Lxvi	**1**	The paper: (**5.g.85**) Andrejević, M., Litovski, V., "*ANN Application In Modelling of Chua's Circuit*", Proc. of Neurel 2002, Belgrade, September 2002, pp. 119-122 (uploaded at http://people.eecs.berkeley.edu /~chua/papers/Litovski02.pdf) is cited: 1. In the paper: Dalkiran, I. Dalkiran, F.Y. Danisman, K. Kilic, R.,, "*Prediction of Dynamics of Chaotic Chua's Circuit with Artificial Neural Network*", SIU 2007. IEEE 15th Signal Processing and Communications Applications, 2007, June 2007, pp. 1-4, Location: Eskisehir.
Lxvii	**4**	The paper: (**5.g.86**) Andrejević, M., Litovski, V., "*Non-Linear Dynamic Network Modelling Using Neural Networks*", Int. Congress on Computional and Applied Mathematics, Leuven,

		Belgium, 22.July-26.July, 2002, pp. 16 was cited: 1. In the paper: Čeperić, V., and Barić, A., "*Conducted electromagnetic emission current source modelling by artificial neural networks*",16th Int. Conf. on Software, Telecommunications and Computer Networks, 2008. SoftCOM 2008, Sept. 2008, pp. 55 – 59, Split, Cratia, ISBN: 978-953-6114-97-9, 2. In the paper: Čeperić, V., and Barić, A., "Modelling of Electromagnetic Immunity of Integrated Circuits by Artificial Neural Networks", 20th Int. Zurich Symposium on Electromagnetic Compatibility, 2009, Jan. 2009, pp. 373 – 376, Zurich, Switzerland, ISBN: 978-3-9523286-4-4. 3. In the PhD thesis: Ackermann, D. W., "*Neural network inference measurements applied to the pebble bed modular reactor*", Thesis (Ph.D. (Electronical Engineering)--North-West University, Potchefstroom Campus, South Africa, 2004. 4. Čeperić, V., Barić, A., Pejčinović, B., "Artificial neural network in modelling of voltage controlled oscillators with jitter", Proc of the 12th IEEE Mediterranean Electrotechnical Conf., 2004. MELECON 2004, May 2004, Dubrovnik. DOI: 10.1109/MELCON.2004.1346871
Lxviii	**12**	The paper: (**5.g.90**) Stefanovic D., Kayal M., Pastre M., Litovski V. B. "*Procedural Analog Design (PAD) Tool*", IEEE ISQED 2003, 4th Int. Symp. on Quality Electronic Design, 24-26 March 2003, San Jose, California, pp. 313-318, was cited: 1.In the paper: Зинченко, Л.А., "*Интеллектуальные системы схемотехнического проектирования*"**,** Десятая национальная конференция по искусственному интеллекту с международным участием, КИИ-2006, Обнинск, 25-28 сентября 2006 года, УДК 621.372. www.raai.org/resurs/papers/kii-2006/seminar/Zinchenko.doc, 2. On the web site: www.grabinski.ch/GMC (wladek@grabinski.ch), "*EKV Modeling Engineering Support*", http://legwww.epfl.ch/ekv/workshop/papers/03_W_Grabinski_1st_WS_NE.pdf. 3. In the PhD thesis: Iskander, R., "*Connaissance et Synthèse en Vue de la Conception et la Réutilisation de Circuits Analogiques Intégrés*", L'Université Paris VI, Spécialité : Informatique et Micro-électronique, 2 Juillet 2008. 4. In the paper: Bucher, M.; Diles, G.; Makris, N., "*Analog performance of advanced CMOS in weak, moderate, and strong inversion*", Proc. of the 17th Int. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Issue Date:

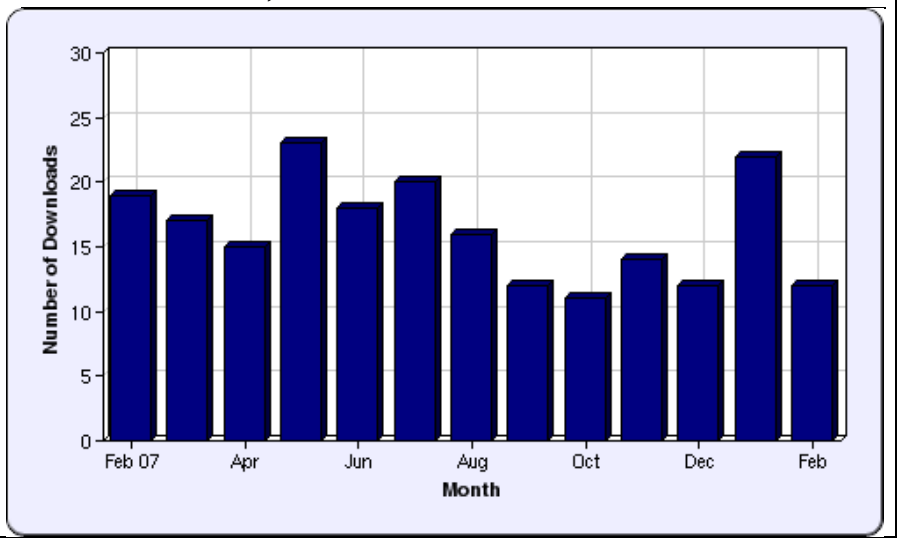
		24-26 June 2010, Warsaw, Poland, Print ISBN: 978-1-4244-7011-2, pp. 54 – 57. 5. In the paper: Youssef, S., Dupuis, D., Iskander R., and Louerat, M.-M., "*Routing Methodology For Nanometric Analog CMOS Devices*", In Proc. of the GDR SOC-SIP, June 2011, Lyon, France. http://www2.lirmm.fr/~w3mic/SOCSIP/images/stories/Routing_Methodology_For_Nanometric_Analog.pdf 6. In the paper: Youssef, S.; Javid, F.; Dupuis, D.; Iskander, R.; Louerat, M., "*A Stack-Based Routing Methodology For Nanometric Analogue CMOS Devices*", In proceedings of the IEEE MOS-AK/GSA Workshop, April 2011, Paris. 7. In the paper: Youssef, S.; Javid, F.; Dupuis, D.; Iskander, R.; Louerat, M., "*A Python-based layout-aware analog design methodology for nanometric technologies*", 2011 IEEE 6th Int. Design and Test Workshop (IDT), Dec. 2011, pp. 62 - 67, Beirut, ISSN: 2162-0601. 8. In the paper: Makris, N., and Bucher, M., "*Temperature scaling of CMOS analog design parameters*", 16th IEEE Mediterranean Electrotechnical Conf. (MELECON), March 2012**,** pp. 187 - 190. 9. In the Master thesis: Sajjadi, A.-S., "*A Computer-Aided Design Tool for Analog Integrated Circuit Building Blocs Realization*", Dept. of Electrical and Computer Engineering, Concordia University, Montreal, Quebec, Canada, 2005. 10. Hamza, A., Philip, A., Ali, M., and Dessouky, M., "*Web-based analog design using tradeoff charts*",19th IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS), Dec. 2012, pp. 13 - 16, E-ISBN :978-1-4673-1259-2 , Print ISBN: 978-1-4673-1261-5 11. Coustans, M., Jazaeri, F., Enz, C., Krummenacher, F., Kayal, M., Meyer, R., Acovic, A., Habaš, P., Lolivier, J., Bucher, M., "*Variability of Low Frequency Noise and mismatch in CORNER DOPED and standard CMOS technology*", Int. Conf. on Noise and Fluctuations (ICNF), June 2017, DOI: 10.1109/ICNF.2017.7985953**,** Vilnius, Lithuania. 12. El-Sisi, and M., Dessouky, M., "*Procedural analog design automation using building block optimization*", IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Dec. 2015, DOI: 10.1109/ICECS.2015.7440351 , Cairo, Egypt.
Lxix	**1**	The paper: (**5.g.98**) Dimitrijević, M., and Litovski, V.,

		"*Implementation of the component characteristic curve tracer using PC-based acquisistion card*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 63-66, was cited 1. In the Master Thesis: Elahe T., Nejad, "*Development Of A Device Characterization Curve Tracer for High Power Application*", Master of Applied Science (MASc), Ryerson University (University place), 2010.
Lxx	**3**	The paper: (**5.g.93**) Andrejević, M., Litovski, V., "*ANN Application in Electronic Diagnosis- Preliminary Results*", Proc. 24th Int. Conf. on Microelectronics (MIEL 2004), Vol. 2, 16-19, pp. 597-600, May 2004, was cited: 1. In the paper: Dubey, P., and Kumar, M., "*An Advanced Automatic Electronic Diagnosis System*", S-JPSET, Vol. 1, No. 1, 2010, pp. 27-31. 2. In the paper: Kumar, Y., "*Electronic Circuits Diagnosis Using Artificial Neural Networks*", Int. J. of Science Engineering and Advance Technology, IJSEAT, August 2015, Vol.3, Issue 8, pp. 393-401. 3. In the paper: V.D. Ivchenko, A.S. Ignatov, P.G. Krug, M.V. Kurakov, S.A. Pavelyev, "*Study of Type I and Type II errors occurring in the automatic fault detection after remote reconfiguration of FPGA of a mobile robot for space application*", International Journal of Control Theory and Applications Vol**.** 9, No. 30, Jan 2016, pp. 61-71
Lxxi	**8**	The paper: (**5.g.94**) V. Litovski, M. Andrejević, M. Zwolinski, "*ANN Based Modeling, Testing, and Diagnosis of MEMS*," IEEE 7th Seminar on Neural Network Applications in Electrical Engineering NEUREL 2004, Sept. 2004, Belgrade, pp. 183-188. 1. In the paper: Sutanto, J., Setia, R., Papania, A., May, G. S., Hesketh, P.J., and Berthelot, Y. H., "Using neural networks to model an electromagnetic-actuated microactuator" J. of Micro/Nanolithography, MEMS and MOEMS , 2007, Vol. 6, No. 1, pp. 13011-13021, the following is cited: 2. In the Master thesis: Zhang, Y., "*Built-In Self-Test Devices and Structures for Mixed Signal Integrated Circuits*", Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, 2006. http://repository.lib.polyu.edu.hk/jspui/bitstream/10397/3887/2/b2069717x_ir.pdf. He says: **"Litovski et al [39] adopted a black box modeling of the non-electronic parts in MEMS devices**

		constructed with artificial neural networks so that new concepts of MEMS simulation, test and diagnosis were introduced to reduce time cost and improve product reliability." 3. In the papaer: Зинченко, Л.А., и Сорокин, Б.С., "*Бионические информационные системы в проектировании микро- и наносистем*", Одинадцатая Национальная Конференция по Искусственному Интеллекту с Международным Участием, г. Дубна, 29 сентября – 3 октября, 2008 года. (Материалы наиболее интересных докладов будут опубликованы в журналах "Искусственный интеллект и принятие решений", "Программные продукты и системы", "Научно-техническая информация" (серия 2).) http://qai.narod.ru/Workshop/zinchenko_cai2008.pdf 4. In the PhD thesis: Deesiri, A., "*Testing and improving Micro accelerometer for Micro Electromechanical Systems (MEMS) design*", Department of Electrical Engineering, Faculty of Engineering, Sripatum University, Bangkok, Thailand, 2008. 5. In the Diploma work: Streit, P., "*Algorithmische Optimierung von Teststrukturen zur Charakterisierung von Mikrosystemen auf Waferebene*", Technische Universitaet Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Professür fuer Mikrosystem- und Gerätetechnik. Den 4. April 2009. 6. In the paper: Ferreira, A., and Aphale, S. S., "*A Survey of Modeling and Control Techniques for Micro- and Nanoelectromechanical Systems*", IEEE Tran. on Systems, Man, and Cybernetics, Part C: Applications and Reviews, May 2011, Vol. 41, No. 3, pp. 350 – 364, ISSN: 1094-6977. 7. In the paper: Lingfei Deng, Vinay Kundur, Naveen Sai Jangala Naga, Muhlis Kenan Ozel, Ender Yilmaz, Sule Ozev, Bertan Bakkaloglu, Sayfe Kiaei, Divya Pratab, and Tehmoor Dar., "*Electrical calibration of spring-mass MEMS capacitive accelerometers*", In Proc. of the Conf. on Design, Automation and Test in Europe (DATE '13), 2013, Grenoble, France, EDA Consortium, San Jose, ISBN: 978-3-9815370-0-0, pp. 571-574. 8. In the Master thesis: Deng, L., "Electrical Stimulus-Based Characterization for Calibration and Testing of MEMS Accelerometer and Gyroscope ", Arizona State University, August 2012.
Lxxii	**9**	The paper: (**5.g.99**) Litovski, V., Andrejević, M, Zwolinski. M. "*Behavioural modelling, simulation, test and diagnosis of MEMS*

using ANNs", In: Proc. Intl. Symp. Circuits and Systems, Kobe, Japan, 2005, pp. 5182-5185, was cited:

1. In the paper: Asgary, R., Mohammadi, K. and Zwolinski, M., "*Using neural networks as a fault detection mechanism in MEMS devices*". Microelectronic Reliability, Vol. 47, No. 1, pp. 142-149,
2. In the PhD thesis: Basheer, N. Z. A., "*An investigation of delay fault testing for multi voltage design*", University of Southampton, Faculty of Engineering, Science and Mathematics, School of Electronics and Computer Science, 2009,
3. In the report: Deesiri , A., **"***Testing and improving Micro accelerometer for Micro Electromechanical Systems (MEMS) design*", Department of Electrical Engineering, Faculty of Engineering, Sripatum University, Year of Publication : B.E. 2008.
4. In the paper: Reimbod, MMP, de Campos, M., Ketzer, M.B., Gerhke, C.S., "*Gray Box Modeling Of Deformable Micro-Nucleus Mems Using Arxmodel And Estimators LS And IV In Bacth***",** Proc. of the 9th Brazilian Conf. on Dynamics Control and their Applications, DINCON'10, Serra Negra, SP - ISSN 2178-3667, pp. 349-355.
5. In the thesis: Reimbold, M. M. P., "*Otimização da síntese do projeto de atuadores MEMS baseados em deformação elástica e estrutura comb-drive*", Universidade Federal do Rio Grande do Sul. Instituto de Física. Programa de Pós-Graduação em Microeletrônica, 2008.



		On the picture the downloading rate from the paper repository of the Southampton university for the year 2007/2008. The title of the picture is: *Dashboard for Litovski, V., Andrejević, M. and Zwolinski, M. (2005)* Behavioral Modelling, Simulation, Test and Diagnosis of MEMS using ANNs. *In: Int. Symposium on Circuits and Systems, 23-26 May 2005, Kobe, Japan.* 6. In the proceedings: Drummond, C. K., and Lisy, F. J., "*Support for microsystems simulation: Are we watching the clock?* " In: Reliability, Packaging, Testing, and Characterization of MEMS/MOEMS VII, edited by Allyson L. Hartzell, Rajeshuni Ramesham, Proc. of SPIE Vol. 6884 68840S-1, 2008, doi: 10.1117/12.764500 7. In the Master thesis: T. M. Starling II, "*Computational Analysis Of Input-Shaping Control of Microelectromechanical Mirrors*", A Thesis Presented to the Graduate School of Clemson University In Partial Fulfillment of the Requirements for the Degree Masters of Science Mechanical Engineering Clemson University, South Carolina USA, August 2008. 8. Bedendo, A., Reimbold, M., Sausen, A.," *Evaluation of Model ARX For Elastic Masses MEMS Using the Indexes RMSE, AIC, and BIC*", J. of Control, Automation and Electrical Systems, April 2014, Vol. 25, Issue 2, pp. 195-205. 9. Dianat, A. ; Attaran, A. ; Rashidzadeh, R., "*Test method for capacitive MEMS devices utilizing pierce oscillator* ", 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 24-27 May 2015, pp. 633 - 636, Lisbon, Portugal, DOI: 10.1109/ISCAS.2015.7168713 .
Lxxiii	**2**	The paper: (**5.g.100**) Dimitrijevic, M., Litovski, V."*Computer integrated analogue electronics laboratory for undergraduate teaching", Proc. of REV 2005 Conf.* Brashov, Romania, proc. on CD, was cited: 1. The paper: Yao, Kai-chao Liao, Chin-wen Chao, Li-ling Lin, Fu-yu, "*Virtual Impedance Analyzer Design and Implementation*", Second Int. Conf. on Innovative Computing, Information and Control, 2007. ICICIC '07. Publication Date: 5-7 Sept. 2007, On page(s): 71-71, Location: Kumamoto, Japan, ISBN: 0-7695-2882-1, 2. The paper: Yao, Kai-chao, "*PC-Based Virtual Bode Analyzer Design And Application In Automatic Measurement Of Filter Manufacturing*", ICIC Express Letters, ICIC Int., ISSN 1881-

		803X, Volume 3, Number 1, March 2009 pp. 33-40.
Lxxiv	**2**	The paper: (**5.g.103**) Dimitrijević,M., and Litovski, V., "*Specific analog electronic circuits analysis using PC-based acquisition card*", IEEE Region 8 EUROCON 2005 Conf., Belgrade, November 21-24, 2005, pp. 910-913, was cited: 1. In the paper: Kai-chao Yao, "*Building PC-base Virtual Signal Generator by Using Labview and XR-2206*", J. of Industrial Education and Technology, Vol. 31. June 2007, pp. 139-152. 2. K Yao, LL Chao, JA Du, FS Chen, "Curriculum Development for Virtual Digital Multi-meter and Measurement to Control in Experiments", ir.ncue.edu.tw
Lxxv	**2**	The paper: (**5.g.104**) Andjelković,M., Litovski, V., and Zerbe, V., "*New aspects in HDL's performance evaluation*", IEEE Region 8 EUROCON 2005 Conf., Belgrade, November 21-24, 2005, pp. 499-502, is cited: 1. The paper: Puthiyottil, S. and Sureshkumar, E., "*Statistical Analysis of Communication Networks with Multidomain Design and Automation Tools*," Second Int. Conf. on Computer Engineering and Applications, 2010, iccea 2010, vol. 2, pp.8-12. 2. Villar, S.A., Rossi, S.R. Acosta, G.G., "*An Approach for Side Scan Sonar Acoustic Images Segmentation using Programmable Logic* ", Latin America Transactions, IEEE (Revista IEEE America Latina), Vol. 13, Issue 5, May 2015, pp. 1478 - 1490, DOI: 10.1109/ TLA.2015.7112005.
Lxxvi	**1**	The paper: (**5.g.106**) Andjelković,M., Litovski, V., and Zerbe, V., "*A Mission Level Design Language Based on Alec++*", Proc. Of the 25th IEEE Int. Conf. On Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, 14-17 May, 2006, pp. 659-662, is cited: 1. Silva, E., , Cavalcante,E., Batista, T., Oquendo, F., Delicato, F.C., Paulo F. Pires, P.F., " *On the Characterization of Missions of Systems-of-Systems* ", proc of the 2014 ACM ECSAW, August 25-29, 2014, Vienna, Austria. http://dx.doi.org/10.1145/2642803.2642829.
Lxxvii	**1**	The paper: (**5.g.107**) Andrejević, M., Litovski, V., and Zwolinski, M., "*Fault Diagnosis in Digital Part of Mixed-Mode Circuits*", Proc. Of the 25th Int. Conf. On Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, 14-17 May 2006, pp. 437-440, is cited: 1. In the paper: Kumar, Y., "*Electronic Circuits Diagnosis Using Artificial Neural Networks*", Int. J. of Science Engineering and

		Advance Technology, IJSEAT, August 2015, Vol.3, Issue 8, pp. 393-401.
Lxxviii	**7**	The paper: (**5.g.108**) Dimitrijević, M., and Litovski, V., «*Power factor and distortion measuring for small loads using USB acquisition module*», Int. Symp. on Remote Engineering and Virtual Instrumentation, REV 2006, Maribor, Slovenia, June 2006. Paper No. SID5.1/2, was cited: 1. In the paper: Yaseen, A.A., »Fast-response power factor computation technique«, 2012 2nd Int. Conf. on Advances in Computational Tools for Engineering Applications (ACTEA), 12-15 Dec. 2012. 2. Chien-Yuan Liu, Chih-Feng Huang, Yann-Chang Huang, "*Electric Power Usage Data Acquisition Module Composed of Two Sensors and a Microcontroller*", Proceedings of the 2nd International Conference on Intelligent Technologies and Engineering Systems (ICITES2013), Lecture Notes in Electrical Engineering Volume 293, 2014, pp 483-489. 3. Gligor, A., Muntean, R., Dumitru, C.-D., "*Digital Solution for Fast Evaluation of the Power Factor in Power Networks*", Scientific Bulletin of the "Petru Maior" University of Targu Mures; Tirgu Mures, Vol. 14, Iss. 1, 2017, pp. 12-16. 4. Králiková, E., Čičáková, O., "Distortion Power Measurements in Education", Measurement 2013, Proc. of the 9th Int. Conf., Smolenice, Slovakia, pp. 75-78. 5. Gligor, A., Dumitru, C.D., Ronay, K., and Muntean, R., "Microcontroller Based Prototype for Reactive Power Compensation in Local Distribution Networks", Procedia Engineering, Vol. 181, 2017, pp. 746-753, open access. 6. Liu J., "*Integration of smart electronics and embedded system teaching internship research and development*", [Information Engineering] research report, 2013, http://ir.csu.edu.tw/handle/987654321/3028 7. Liu J., "*Design of Embedded Wisdom Control Experiment System*", [Information Engineering] research report, 2016, http://ir.csu.edu.tw/handle/987654321/3088.
Lxxix	**5**	The paper: (**5.g.109**) Andrejević, M., and Litovski, V., «*Fault diagnosis in digital part of sigma-delta converter*», Proceedings of the 8th Seminar on Neural network application in electrical engineering, NEUREL ' 2006, pp. 177-180, was cited: 1. In the paper: Kumar, Y., "*Electronic Circuits Diagnosis Using Artificial Neural Networks*", Int. J. of Science Eng. and Advance Technology, IJSEAT, August 2015, Vol.3, Issue 8,

		pp. 393-401. 2. In the PhD thesis: Cai, H., "*Reliability of Analog-to-Digital Sigma-Delta Converters*", Electronics. Telecom Paris-tech, 2013. English. <tel-01171598> https://hal.archives-ouvertes.fr/tel-01171598/file/Cai_PhDthesis_TPT0046.pdf 3. Ferreira, P.M., Cai, H., Naviner, L., **"***Reliability Aware AMS/RF Performance Optimization***",** in Fakhfakh, M., Tlelo-Cuautle, E., and Fino, M. H., **"***Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design*"**,** IGI Global, October, 2014, ISBN13: 9781466666276. 4. Wei, C., Changjiang, F., and Guabao, D., "*Design and Realization of Boundary Scan Experiment System Based on Single chip*", Computer Measurement and control, Vol. 17, No. 8, pp. 1476-1478. 5. Che Bin Fan Xiaoya, "*Testability Design for SoC Based on IDDQ Scanning*", COMPUTER MEASUREMENT & CONTROL, 2009, Vol. 17 No. 8.
Lxxx	**3**	The paper: (**5.g.110**) Litovski, V., Andrejević, M., and, Nikolić, M., «*Chaos based analog-to-digital conversion of small signals*», Proceedings of the 8th Seminar on Neural Network Application In Electrical Engineering, NEUREL ' 2006, pp. 173-176, was cited: 1. In the paper: Zhen Qiang Huang, Wen Li Zhao, Zhi Gang Wang, " *Research on Weak Signal Amplification Principle Based on Parabola Map*", Advanced Materials Research (Volumes 139 - 141), Volume: Manufacturing Engineering and Automation I, pp. 1963-1966, October, 2010, DOI 10.4028/ www.scientific.net/AMR.139-141.1963, 2. In the paper: Che Bin, Fan Xiaoya, "*Testability Design for SoC Based on IDDQ Scanning*", Computer Measurement & Control, Vol. 17, No. 8, 2009, http://d.wanfangdata.com.cn/periodical_jsjzdclykz200908006.aspx. 3. In the paper: Cui Wei, Feng Changjiang, Ding Guobao, "*Design and Implementation of Boundary Scan Test System Based on Single Chip*", Computer Measurement & Control, Vol. 17, No. 8, 2009, http://d.wanfangdata.com.cn/periodical_jsjzdclykz200908007.aspx
Lxxxi	**4**	The paper: (**5.g.111**) Anđelković, B., Dimitrijević, M.,, and Litovski, V., "*Using Grid Computing in Parallel Electronic Circuit Simulation*," Proceedings of Electronics' 2007, Sozopol, Bulgaria, September 2007, book 4, pp. 109-114, was cited: 1. In the paper: Zhuang, H., He, F., Lin, X., Zhang, L., Zhang, J.

		Zhang, X., and Chan, M., „*A Web-Based Platform for Nanoscale Non-Classical Device Modeling and Circuit Performance Simulation*", 2009 Int. Conf. on Web Information Systems and Mining, the following was cited: 2. This paper is offered at "*The MIT Press Beowulf Cluster Computing 2*" at the site: http://www.toodoc.com/The-MIT-Press-Beowulf-Cluster-Computing-2-pdf.html 3. In the paper: А. І. Петренко, В. В. Ладогубець, О. Д. Фіногенов, Б. В. Булах, "*Дослідження архітектури комплексу схемотехнічного моделювання GRIDALLTED*", Вісник Університету «Україна» № 2, 2011, Розділ 2, Комп`ютерні системи, мрежі, та ї компоненти. GRID Системи, pp. 65-70. 4. Hao Zhuang, Jin He , Wanling Deng, Xiangyu Zhang, Xiaoan Zhu, Qingxin He, Mansun Chan, "*A Web-Based Education Platform for nanoscale device modeling and circuit simulation*", 4th Interdisciplinary Engineering Design Education Conf. (IEDEC), March 2014, pp. 84 - 87, Print ISBN: 978-1-4799-4381-4.
Lxxxii	**1**	The paper: (**5.g.114**) Andrejević, M., and Litovski, V., „*Hierarchical Approach To Diagnosis Using ANNs* ", Proc. 26th Int. Conf. On Microelectronics (Miel 2008), Niš, Serbia, 11-14 May, 2008, pp. 395-398, was cited: 1. The thesis: A Kavithamani, A., "*Certain new approaches to fault diagnosis of analog electronic circuits using frequency response methods*" Anna University, Faculty of Electrical and Electronics Engineering, 2014, http://hdl.handle.net/10603/24732.
Lxxxiii	**3**	The paper: (**5.g.115**) Sokolović, M., Petković, P., and Litovski, V., "*Design for Testability for SoC Based on IDDQ Scanning*", Proc. 26th Int. Conf. On Microelectronics (Miel 2008), Niš, Serbia , 11-14 May, 2008, pp. 407-410, is cited: 1. In the paper: Abdullah, F., Nayan, N., Jamil, M.M.A., and Kamsin, N. , "*IDD scan test method for fault localization technique on CMOS VLSI failure analysis*", 2010 IEEE Int. Conf. on Semiconductor Electronics (ICSE), 28-30 June 2010, Melaka, Malezya, Print ISBN: 978-1-4244-6608-5, pp. 104 – 107. 2. Guibane, B., and Hamdi, B., "DFT for Analog and Mixed Signal IC Based on IDDQ Scanning", MIXDES 2012, 19 the Int. Conf. "Mixed Design of Integrated Circuits and Systems", May 24-26, 2012, Warsaw, Poland, pp. 431-435

		3. Guibane, B., and Hamdi, B., and MTIBAA,A., ”A Novel Iddq Scanning Technique For Pre-Bond Testing”, Int. J. of Applied Engineering Research ISSN 0973-4562 Vol. 11, Number 8 (2016) pp 5781-5786
Lxxxiv	**1**	The paper: (**5.g.116**) Milojković, J. and **Litovski, V.,** “*Comparison of Some ANN Based Forecasting Methods Implemented on Short Time Series*”, 9th Symposium on Neural Network Applications in Electrical Engineering, NEUREL-2008, Belgrade, 2008, pp. 179-179, was cited: 1. Zhong, C., Guo, T., Jiang, Z., Liu, X., and Chu, X., “*A hybrid model for water level forecasting: A case study of Wuhan station*”, 4th Int. Conf. on Transportation Information and Safety (ICTIS), Aug. 2017, DOI: 10.1109/ICTIS.2017.8047772, Banff, AB, Canada.
Lxxxv	**1**	The paper: (**5.g.124**) Milojković, J., Bojanić, S., and Litovski, V., “*On Prediction in Electronics*”, Proc. 27th Int. Conf. on Microelectronics (MIEL 2010), Niš, Serbia, 16-19 May, 2010, pp. 275-278, was cited: 1. In the paper: Gnibba-Yukawa, K., Decker, R., “*Comments on the Model Testing by Goodwin and Meeran (2012): Comparison of the Utility-based and the Gomperty Curve Approach for High-technology Product Sales Forecasting*”, J. of Product Innovation Management, http://dx.doi.org/10.1111/j.1540-5885.2012.00965.x DOI - 10.1111/j.1540-5885.2012.00965.x.
Lxxxvi	**1**	The paper: (**5.g.127**) Andrejević Stošović, M., and Litovski, V., ” *Hierarchical Approach to Diagnosis of Electronic Circuits using ANNs* ”, 10th Symposium on Neural Network Application in Electrical Engineering, NEUREL-2010, Faculty of Electrical Engineering, University of Belgrade, Serbia, September 2010, ISBN 978-1-4244-8818-6, pp. 117-122, was cited: 1. Mohamed, A.H., "*Diagnostic Neural Network Systems for the Electronic Circuits* ", Arab J. of Nuclear Science and Applications, Vol. 47, No. 3, pp. 16-23, 2014.
Lxxxvii	**1**	The paper: (**5.g.128**) Milojković, J., Litovski, V., Nieto-Taladriz, O., and Bojanić, S., “*Forecasting Based on Short Time Series Using ANNs and Grey Theory – Some Basic Comparisons*”**,** In Proc. of the 11th Int. Work-Conf. on Artificial Neural Networks, IWANN 2011, June 2011, Torremolinos-Málaga (Spain). J. Cabestany, I. Rojas, and G. Joya (Eds.): Part I, LNCS 6691, pp. 183–190, 2011,

		© Springer-Verlag Berlin Heidelberg 2011. ISSN: 0302-9743, was cited: 1. In the PhD thesis: Yao, Y., "*The Water Situation of the Future Mega City "Urumqi" (NW-China)–Resources, Risk, Conservation and Management*", Dissertation, Naturwissenschaftlich-Mathematischen Gesamtfakultät, Ruprecht-Karls-Universität Heidelberg, 2013.
Lxxxviii	**3**	The paper: (**5.g.129**) Milić, M., Andrejević Stošović, M., Litovski, V., "*Oscillation Based Analog Testing - A Case Study*", 34th Int. Convention on Information and Communication Technology, Electronics and Microelectronics- MIPRO 2011, Opatija, Croatia, 2011, Vol. 1, pp. 118-123, ISBN 1847-3938, was cited: 1. In the paper: Arbet, D.; Stopjakova, V.; Majer, L.; Gyepes, G.; Nagy, G., "*New OBIST Using On-Chip Compensation of Process Variations Toward Increasing Fault Detectability in Analog ICs*," *IEEE Transactions on Nanotechnology*, vol.12, no.4, pp. 486,497, July 2013, doi: 10.1109/TNANO. 2013.2251656. 2. Ojha, M.K., and Akashe, S., "Analog and Mixed Signal Test Method based on OBIST Technique", Int. J. of Computer Applications (0975–8887), Vol. 109, No. 5, Jan. 2015, pp. 33-37. 3. Ojha, M.K., and Akashe, S., "Test Method for Analog and Mixed Signal Device based OBIST and IDDQ", Int J. of Computer Applications (0975–8887), Vol. 112, No. 1, Feb. 2015, pp. 38-44.
Lxxxix	**2**	The paper: (**5.g.132**) Andrejević Stošović, M., Lukač, D., Litovski, V**.**, "*Realistic modeling and simulation of the PV system - converter interface*", Proceedings of the 4th Small Systems Simulation Symposium, Niš, 2012, ISBN 978-86-6125-059-0, pp. 28-32, was cited: 1. Gupta, A., Kumar, P., Pachauri, R.P., Chauhan, Y.K., "*Effect of Environmental Conditions on Single and Double Diode PV System : A Comparative Study*", Int. J. of Renewable Energy Research, Vol.4, No.4, 2014, pp. 849-858. 2. Gupta, A., and Chauhan, Y.K., "*Detailed performance analysis of realistic solar photovoltaic systems at extensive climatic conditions*", Energy, Vol. 116, Part 1, 1 Dec. 2016, Pages 716-734.
xC	**1**	The paper: (5.g.135) Dimitrijević, M., and Litovski, V., "*Quantitative Analysis of Reactive Power Definitions for Small*

		Non-linear Loads", Proceedings of the 4th Small Systems Simulation Symposium, Niš, 2012, ISBN 978-86-6125-059-0, pp. 150-154, was cited: 1. Taha, M. H., "*Single phase series active filter load compensation for aircraft applications*", 16th Int. Power Electronics and Motion Control Conference and Exposition (PEMC), Sept. 2014, DOI: 10.1109/EPEPEMC.2014.6980533**,** Antalya, Turkey
xCi	**1**	The paper: (5.g.137) Milojković, J., Litovski, I., and Litovski, V., "*ANN Application for the Next Day Peak Electricity Load Prediction* ", Proc. of the 11th Symp. on Neural Network Application in Electronic Engineering, NEUREL 2012, Belgrade, Sept. 2012, pp. 237-241, was cited: 1. Varshney, S., Verma, T., "*Half Hourly Electricity Load Prediction using Echo State Network*", Int. J. of Science and Research (IJSR), Vol. 3, No. 6, June 2014, ISSN (Online): 2319-7064, Paper ID: 02014351.
xCii	**1**	The paper: (5.g.138) Andrejević Stošović, M., Lukač, D., Litovski, I., and Litovski, V., "*Frequency Domain Characterization of a Solar Cell*", Proc. of the 11th Symp. on Neural Network Application in Electronic Engineering, NEUREL 2012, Belgrade, Sept. 2012, pp. 259-264, was cited 1. Zixiong Wang, Tsonev, D. ; Videv, S. ; Haas, H., "*On the Design of a Solar-Panel Receiver for Optical Wireless Communications With Simultaneous Energy Harvesting*", Published in:IEEE Journal on Selected Areas in Communications, Vol. 33, Issue 8, pp. 1612-1623, DOI:10.1109/JSAC.2015.2391811, January 2015.
xCiii	**1**	The paper: (**5.g.148**) Mirković, D., Petković, P. and Litovski, V., "Experience in Using Open Command Environment for Analysis in Education", Proc. of 1st Int. Conf on Electrical, Electronic and Computing Engineering IcETRAN 2014, Vrnjačka Banja, Serbia, June 2 – 5, 2014, ISBN 978-86-80509-70-9, pp. ELI 1.8.1-5, was cited 1. In the PhD thesis: David Černý, "Algorithms for Analysis of Nonlinear High-FrequencyCircuits", Czech Technical University in Prague, Faculty of Electrical Engineering 13137 Department of Radioelectronics, 2016.
xCiv	**1**	The paper: (**5.h.41**) Litovski, V., et al.: "*Analysis of bipolar and MOS circuits using program MOST*", Proc. of 16th Yugoslav Conf. on Microelectronics, MIEL 88, Zagreb, 1988, pp. 303-310. (In

		Serbian) was cited 1. In the paper: Melikian, V., "Logic *Simulation of Digital Circuits Exposed to Radiation*", Facta Universitatis, Series: Electronics and Energetics, Vol. 12, No.1, 1999, pp. 71-86, UDC 621.3.049.7.
xCv	**5**	The paper: (**5.h.50**) Ž. Mrčarica, V. B. Litovski, M. Jakovljević, H. Detter, "*Hierarchical modelling of microsystems in an object-oriented HDL*", Proc. of the 21st Int. Conf. On Microelectronics, MIEL'97, Niš, Yugoslavia, September 1997, pp. 475-478, was cited: 1. In the paper: Zhang, T. **(Cadence Design Systems, Inc., Cary, NC 27511 USA.**), Chakrabarty, K., and Fair, R.B., "*Behavioral modeling and performance evaluation of microelectrofluidics-based PCR systems using SystemC*", IEEE Trans. on CAD of Integrated circuits and Systems, Vol. 23, No. 6, June 2004, pp. 843-858. It is written: "**We adopt the strategy of trading-off behavioral fidelity with the efficiency of analysis, "blinding" unnecessary low-level detail, and paying more attention to certain tractable subsystems [42].** " As (the last) [42] the following is cited: 2. In the book: Zhang, T., Chakrabarty, K. and Fair, R. B., "A Hierarchical Design Platform for Microelectrofluidic Systems (MEFS)", Springer US, 2006, ISBN 978-0-387-24520-1 (Print) 978-0-387-25786-0 (Online), and in the papers: 3. In the book: Zhang, T., Chakrabarty, K., Fair, R.B., "*Microelectrofluidic Systems: Modeling and Simulation*", CRC Press, 2002, ISBN: 9780849312762 4. In the paper: Mackerle, J., "*Object-oriented techniques in FEM and BEM A bibliography (1996-1999)*", Finite Elements in Analysis and Design, Vol. 36, 2000, pp. 189-196. 5. In the paper: Mackerle, J., "*Object-oriented programming in FEM and BEM: a bibliography (1990–2003)*", Advances in Engineering Software, Volume 35, Issue 6, June 2004, Pages 325–336
xCvi	**3**	The paper: (**5.h.98**) Dimitrijević, M., Litovski, V., Jovanović, S., "*Computer system for laboratory exercises in electronics*"**,** *Proc. of 5th Conf. of Indel*, Banja Luka, B&H, pp. 156-160, 2004, in Serbian, was cited: 1. In the paper: Yao, Kai-chao Liao, Chin-wen Chao, Li-ling Lin, Fu-yu, "*Virtual Impedance Analyzer Design and Implementation*", Second Int. Conf. on Innovative Computing, Information and Control, 2007. ICICIC '07. Sept. 2007, pp. 71-

		71, Location: Kumamoto, Japan, ISBN: 0-7695-2882-1, 2. In the paper: Yao, Kai-chao, "*PC-Based Virtual Bode Analyzer Design And Application In Automatic Measurement of Filter Manufacturing*", ICIC Express Letters, ICIC Int., ISSN 1881-803X, Volume 3, Number 1, March 2009 pp. 33-40. 3. In the paper: * Милисављевић, Ј., Поповић, А.,"*Сет наставних комплета "Физика помоћу рачунара"*", Републички семинар о настави физике 2006, Beograd, pp. 1-4.
xCv	**3**	The paper: (**5.h.108**) Andrejević, M., Petrović, V., Mirković, D., and Litovski, V. B.,: «*Delay defects diagnosis using ANNs*», L Konferencija ETRANa, Belgrade, June 2006, pp. EL, 1, 27-30, was cited: 1. In the paper: Cui Wei, Feng Changjiang, Ding Guobao, "*Design and Implementation of Boundary Scan Test System Based on Single chip*", Computer Measurement & Control, Vol. 17, No. 8, 2009. 2. In the paper: Che Bin, Fan Xiaoya, "*Testability Design for SoC Based on IDDQ Scanning*", Computer Measurement & Control, Vol. 17, No. 8, 2009, http://d.wanfangdata.com.cn/periodical_jsjzdclykz200908006.aspx. 3. Kumar, Y., "*Electronic Circuits Diagnosis Using Artificial Neural Networks*", Int. J. of Science Engineering and Advance Technology, IJSEAT, August 2015, Vol.3, No. 8, pp. 393-401.
xCvi	**1**	The paper (**5.h.113**) Andrejević, M., and Litovski, V., «*Fault diagnosis in analog part of mixed-mode circuits*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 117-120, was cited: 1. In the paper: Kumar, Y, "*Electronic Circuits Diagnosis Using Artificial Neural Networks*", Int. J. of Science Engineering and Advance Technology, IJSEAT, August 2015, Vol.3, Issue 8, pp. 393-401.
xCvii	**2**	The paper: (**5.h.116**) Anđelković, B., Litovski, V. B., and Petković, P., «*Implementation and performance analysis of parallel circuit simulator on BEOWULF cluster*», 51. Konferencija Za Elektroniku, Telekomuniklacije, Računarstvo, Automatiku i Nuklearnu Tehniku, ETRAN, Herceg Novi, 04-08 Jun, 2007, Rad. EL1.6, is cited: 1. In the paper: Ruey-Kuen Perng, Tien-Hsiung Weng, Kuan-Ching Li, "*On Performance Enhancement of Circuit Simulation Using Multithreaded Techniques*,", 12th Int. Conf. on Computational Science and Engineering, CSE'09, Vancouver,

		Canada, 2009, Vol. 1, pp.158-165. 2. In the paper: Tien-Hsiung Weng, Ruey-Kuen Perng, and Kuan-Ching Li, "*On parallelization of circuit simulation SPICE3 using multithreaded programming techniques*", J. of the Chinese Institute of Engineers, Volume 35, Issue 2, 2012, pp. 259-267.
xCviii	**1**	The paper: (**5.h 152**) Lukač, D., Andrejević Stošović, M., Milovanović, D., and Litovski, V., "*Reference Analysis of the Analogous Models for Photovoltaic Cells by Comparison with the Real Photovoltaic Modules*", X Int. Symp. on Industrial Electronics INDEL 2014, Banja Luka, November 06_08, 2014,pp. 235-240, was cited in: 1. In the PhD thesis: Abreu, E.F.M., "Avaliação do Recurso Solar e Modelação de um Sistema de Energia Fotovoltaica Ligado à Rede Elétrica da Ilha da Madeira", Universidade de Évora, Escola De Ciências E Tecnologia, Departamento De Fisica, 2016.
iC	**118**	The book: (**9.14**) Litovski, V., Zwolinski, M., *"VLSI Circuit Simulation And Optimization"*, Chapman and Hall, London, 1997, was cited in: 1. Chappel, B., "*The fine art of IC design*", IEEE Spectrum, Vol. 36, No. 7, July 1999., pp. 30-34, (Special issue of the IEEE Spectrum, devoted to the future chip with 100 million transistors.) is written: **"For background reading, a textbook that starts at the basics and covers the basic solution methods used in most modern CAD capabilities is *VLSI circuit simulation and optimization* by, V. Litovski and M. Zwolinski ...". Madam Chappel "is a principal engineer with Intel Corp.'s Technology Department within the Microprocessor Products Group in Hilsboro, Ore., where she has been since 1995. For 17 years prior that, she was a member of the research staff at IBM Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N.Y ...".**

IEEE SPECTRUM

http://www.spectrum.ieee.org

The 100-million transistor IC Design Fabrication

JULY 1999 VOLUME 36 NUMBER 7

To probe further

For background reading, a textbook that starts at the basics and covers the basic solution methods used in most modern CAD capabilities is *VLSI Circuit Simulation and Optimization*, by **V. Litovski** and **M. Zwolinski** (Kluwer Academic, Dordrecht, the Netherlands, 1997).

About the author

Barbara Chappell is a principal engineer with Intel Corp.'s Design Technology Department within the Microprocessor Products Group in Hillsboro, Ore., where she has been since 1995. For 17 years prior to that, she was a member of the research staff at IBM Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N.Y. Chappell has produced more than 24 publications and has been issued more than 18 U.S. patents.

The fine art of IC design

BARBARA CHAPPELL
Intel Corp.

2. Dreyer, A., "*Interval Methods for Analog Circuits*", Berichte des Fraunhofer ITWM, Nr. 97 (2006) Fraunhofer-Institut für Techno- und Wirtschaftsmathematik ITWM, 2006, ISSN 1434-9973, (as the first reference!) and in
3. Dreyer, A., "*Interval Analysis of Linear Analog Circuits*", 12th GAMM - IMACS Int. Symposium on Scientific Computing, Computer Arithmetic and Validated Numerics, 2006. SCAN 2006, Publication Date: 26-29 Sept. 2006, On page(s): 14-14, Location: Duisburg, Germany, ISBN: 978-0-7695-2821-2.
4. A. Dreyer, "*Resolving Parameter Dependences for Interval Analysis of Linear Analog Circuits*", Proc. 9th Int. Workshop on Symbolic Methods and Applications in Circuit Design (SMACD 2006), Florence, Italy, Oct. 2006.
5. In the curriculum: TECHNION (Israel Institute of Technology, Haifa, Israel) at the "Computer Science Department", on the teaching subject"Algorithmic Aspects in VLSI Design (CS

		236604)" lead by Dr. Israel Wagner, as a compulsory literature the above is listed (http://www.cs.technion.ac.il/~wagner/pub/aav.html). 6. In the curriculum: Technische Universitaet Hamburg-Harburg (TUHH) department "Arbeitsbereit Mikrosystemtechnik", within the postgraduate studies curriculum: "Simulation in der Mikrosystemtechnik", in the chapter "5. System simulation" of the textbook http://www.tu-harburg.de/mst/ is written: **"Subsequently, the operation and algorithmic framework of analog simulation is represented, oriented on the widespread network simulator SPICE [8, 11]. The fundamental techniques can be transferred to most analog simulators".** Reference is the above. 7. In the curriculum: National University of Ireland, Galway, within the curriculum for the subject: "*VHDL for: ASIC design capture, verification and synthesis", within the section "booklist*", the above it is recommended. (http://www.ee.nuigalway.ie). 8. In the curriculum: Technische Univerzitaet in Kiel, Germany, on the chair: "*Algemeine und Teoretische Electrotechnik*" within the subject "Praktikum Schaltungsimulation", Prof. Neumann, I., et. all., in the literature recommend the above. 9. In the curriculum: The Technische Universitaet Graz, for the subject "*Die matematische Methoden in SPICE*", www.ife.tugraz.at/Elektronik/ Roehrer/Simulation/math.pdf 10. In the curriculum: University of Ulm, for the subject "*Circuit Simulation and Optimization*", at master studies of electrical engineering, thought by Prof. Dr. Volker Schmitt. http://www-crypto.htw-saarland.de/cgi-bin/moduldb-c?bkeys= em&ckeys= esuo&lang=en, 11. In the curriculum: The University of Southampton, England, within the subject: *Design Automation*, Prof. A. Brown, recommends: Litovski, V., Zwolinski, M.: *VLSI Circuit Simulation and Optimization*. Chapman and Hall, London, 1997. (https://secure.ecs.soton.ac.uk/ug/handbook/99/Units/el325.html). 12. Swarthmore College, Great Britain, Prof. Erik Cheever, prepared a textbook posted on the web. In the chapter: "An Algorithm for Modified Nodal Analysis" is written: "Many of the ideas and notations from this page are from Litovski, thought the discussion here is quite simpler because only independent voltage and current sources are considered". (http://www.swarthmore.edu/NatSci/echeeve1/Ref/mna/ MNA3.html).

		13. In the curriculum: Hochschule für Technik und Wirtschaft des Saarlands, Goebenstraße 40, 66117 Saarbrücken, in the curriculum is written: Modulbeschreibung: Titel des Moduls: Schaltungssimulation und Optimierung, Literatur: as above! 14. In the curriculum: National Institute of Technology, Karnataka, Surathkal, India, within the subject:" Modeling and Simulation (3-0-0) 3", at: Department of Electronics & Communication Engineering, as a basic literature as bove is recommended. 15. In the curriculum: Manchester Metropolitan University, Faculty of Science and Engineering, Department of Engineering, in the curriculum is written: Postgraduate Network in Advanced, Subject area: H610 Electronic Engineering, Unit title: *Electronic Circuit Design*, Unit code number: 64ET4505, Unit leader(s) Mr. L.Travis, Dr. F.J.Swift, Indicative student learning resources: as above. 16. In the curriculum: Technische Universitaet Graz, Institut fuer Elektronik, in the curriculum is written: Lehrversnstaltungen, Schaltungssimulation, Matematische metoden in der Schaltungssimulation, SSIM VO. 2005, ...Referenzen, [3] as above. *http://www.ife.tugraz.at/Elektronik/Soeser/Simulation/SSIM_mathematische_Methoden.pdf* 17. In the curriculum: Ecole Nationale Supérieure des Télécommunications, Département COMELEC , Prof. Hervé Petit, for the subject: "*Introduction à la simulation électrique*" recommandas: [1] C.W. Ho, A.E. Ruehli et A. Brennan : *The Modified Nodal Approach to Network Analysis*. IEEE Transactions on circuits and systems, juin 1975. [2] V. Litovski et M. Zwolinski : *Circuit Simulation and Optimisation*. Chapman & Hall, 1997. [3] J-P. Nougier : *Méthodes de calcul numérique*. Hermes, 2001. [4] SPICE, http://bwrc.eecs.berkeley.edu/Classes/IcBook/SPICE/. 18. In the curriculum: "Metropolitan University (MU) at Sylhet, Bangladesh", for "B.Sc. Engineering in Electronics & Telecommu-nication Engineering (ETE)" as a literature for the subject "*Very Large Scale Integration (VLSI)*". 19. ESTIA: Ecole Superieure des Technologies Industrielles Avancees, (64102 Bayonne Cedex, France) in the application for the doctoral thesis of Frederic Seyler having the title: *"Conception et prototypage d'un simulateur de circuit electrique a partir du schema de principe du circuit (extensible aux circuit hydrauliques et pneumatiques)"*, as the first reference is cited the

		above. (http://www.estia.fr/čncouture/last_sujet.html). (http://dept-info.labri.u-bordeaux.fr/~maylis/DEA/sujet1.html). 20. In the master thesis: Li Zheng, "*A Distributed Environment for the Simplification of Multiple Boolean Functions*", the University of East Anglia, Norwich, England, October 1997. *http://www. itr.unisa.edu.au/člzheng/MSC_Li.pdf*, 21. In the master thesis: Lakshminarayanan, C. C., "*An Analog kernel using direct method for solving ordinary differential-algebraic equations in a Mixed-mode Simulator*", University of Sinsinnati, Deparment of Electrical and Computer Engineering and Computer Science of College of Engineering, USA, December 1997. 22. In the PhD thesis: Ingo Naumann, "*Sortierverfahren und Datenstrukturen in der VLSI-Netzwerksimulation*", Technischen Fakultät der Christian-Albrechts-Universit¨at zu Kiel, Kiel 2003. 23. In the PhD thesis: Chen-Wei Liu, *"Floorplan and Power/ Ground Network Co-Synthesis for Fast Design Convergence*", Graduate Institute of Electronic Engineering, National Taiwan University, 2005. 24. In the PhD thesis: Chandankumar Reddy Karrem, "*Trust-tech based methods for optimization and learning*", Faculty of the Graduate School of Cornell University, USA, May 2007 25. In the paper: Chen-Wei Liu (Synopsys Taiwan Limited) and Yao-Wen Chang "*Floorplan and Power/Ground Network Co-Synthesis for Fast Design Convergence*", Int. Symposium on Physical Design, ISPD'06, April 9–12, 2006, San Jose, California, USA. 26. In the paper: Liu, C.-W., and Chang, Y.-W., " *Power/Ground Network and Floorplan Cosynthesis for Fast Design Convergence*", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, VOL. 26, NO. 4, APRIL 2007, pp. 693-704. 27. In the PhD thesis: Albustani, H., "*Modelling Methods for Testability Analysis of Analog Integrated Circuits Based on Pole-Zero Analysis*", Der Fakultät für Ingenieurwissenschaften der Universität Duisburg-Essen zur Erlangung des akademischen Grades eines Doktor-Ingenieur (Dr.-Ing.) vorgelegte Dissertation. Referent: Prof. Dr.-Ing. Axel Hunger, Korreferent: Prof. Dr-.Ing. Bernd Straube, Tag der mündlichen Prüfung: 06 August 2004

		28. In the PhD thesis: Sung-Hwan Min, "*Automated Construction of Macromodels from Frequency Data for Simulation of Distributed Interconnect Networks*", at: School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2004. 29. In the paper: -J. Haase (Fraunhofer-Institut für Integrierte Schaltungen, Außenstelle EAS Dresden), W. Vermeiren, Clauss, C., und P. Schwarz, "*Erste Erfahrungen mit der simulation von Mixed-Signal-Schaltungen mit einem VHDL-AMS-Simulator*", ASIM-Tagung, Simulationstechnik, Weimar, 17.09. 1999, Praxisforum, pp. 33-38. 30. In the paper: -J. Haase, P. Schwarz, P.Trappe und W. Vermeiren, "*Erfahrungen mit VHDL-AMS*", HDL-Workscop, Jena, 25. 11.1999, pp. 29-34. 31. In the paper: -J. Haase, P. Schwarz, P.Trappe und W. Vermeiren, "*Erfahrungen mit VHDL-AMS bei der Simulation heterogener Systeme*", ITG/GI/GMM Workshop, "Methoden und beschreibungssprachen zur modellirung und verifikation von Schaltungen und Systemen", Frankfurt/M, 28-29.02.2000, pp. 167-175, where the following is claimed: "**Bei der beschreibung analog-digitaler Teilsysteme ist der definierte mixed-mode-Simulationszyklus zu berueksichtigen [9]** where [9] is the above book. 32. In the paper: Rafael López-Ahumada and Rafael Rodríguez-Macías, "*A Strategy for Rapid Mismatch Evaluation of Transient Characteristics of CMOS Analog Cells*", Analog Integrated Circuits and Signal Processing, Kluwer, Vol. 37, No. 2. Nov. 2003, pp. 103-111, 2003, ISSN: 0925-1030. 33. In the paper: Chen, T.-H., Tsai, J.-L., Chen, C. C.-P., Karnik, T., "*HiSIM: Hierarchical Interconnect-Centric Circuit Simulator"*, Proc. of the IEEE ICCAD 2004, November 2004. 34. In the paper: Shwehdi, M. H., et all., "*A parametric sensitivity formulation for power system analysis*", Proc. of the 14th Power sys-tems computation Conf.", 14th PSCC, Sevilla, 24-28, June 2002, Session 09, Paper 1, Page 1-7, 35. In the paper: Brown, A.D., Ross, J.N., and Nichols, K.G. "*Time-domain simulation of mixed nonlinear magnetic and electronic systems*", IEEE Trans. on Magnetics**,** Volume: 37, Issue: 1, Part 2, On page(s): 522-532, Jan 2001, ISSN: 0018-9464. 36. In the paper: Y.-W. Chang, T.-C. Chen, and H.-Y. Chen,

		"*Physical Design for System-On-a-Chip*" in Essential Issues in SOC Design (Y.-L. Lin, Editor), Springer, pp. 311-403, 2006 (invited article). 37. In the paper: Kato, S. Hoshi, N. Oguchi, K., "*Analysis of power electronics systems including cascaded induction machines with modified nodal analysis*", Proceedings of the Power Conversion Conf., 2002. PCC Osaka, Japan, Volume: 1, pp: 282-287, ISBN: 0-7803-7156-9. They say: "**In the modified nodal analysis method, matrix stamps [5] can easily compose the matrix equations used for obtaining solutions.. "** 38. In the paper: Damper, R.I., French, R.L.B., and Scutt, T.W., "The Hi-noon neural simulator and its applications", Microelectronics Reliability, Vol. 41, pp. 2061-2065, 2001. 39. In the paper: Blaabjerg, F., Chiarantoni, E., Del L'Aquila, A., Liserre, M., and Vergura, S., "*Sensitivity analysis of an lcl-filter-based three-phase active rectifier via a "virtual circuit" approach*", J. of Circuits, Systems, and Computers, Vol. 13, No. 4, 2004, pp. 665-686. 40. In the paper: Kato, S., Hoshi, N., Oguchi, K., "*Brushless slip-power recovery system simulation using modified nodal approach*", IEEJ Trans. IA, Vol. 124, No. 12, 2004, pp. 1252-1260. 41. In the paper: Naumann, I., and Dirks, H.K., "*Efficient reordering for direct methods in analog circuit simulation*", Electrical Engineering, Vol. 89, No. 4, March 2007, Pages 333-337**.** 42. In the paper: Cheever, E., "*Demystifying spice: Generating and solving circuit equations symbolically*", Computers in Education Journal, Volume 14, Issue 1, January 2004, Pages 30-37. 43. In the paper: Wan, B., Richard Shi, C.-J.**, "** *Hierarchical multi-dimensional table lookup for model compiler based circuit simulation*", Proceedings - Design, Automation and Test in Europe Conf. and Exhibition , Volume 2, 2004, Pages 1310-1315**.** 44. In the paper: Sun, W., Chen, R.M.M., Jiang, Y.-L., "*Tolerance analysis for electronic circuit design using the method of moments*", Proceedings - IEEE Int. Symposium on Circuits and Systems, Volume 1, 2002, Pages I/565-I/568**.** 45. In the paper: Legrand, F., et all., "*Simul'Elec, a Delphi written simulator for power Electrical Engineering, using VHDL-AMS modeling*", IEEE Int. Behavioral Modeling and Simulation Workshop, 2007. BMAS 2007, Publication Date: 20-21 Sept.

2007, On page(s): 94-99, Location: San Jose, CA, USA, ISBN: 978-1-4244-1567-0

46. In the book: Chang, Y.-W., Chen, T.-C., and Chen, H.-Y., "*Physical Design for System-On-a-Chip*", http://cc.ee.ntu.edu.tw/~ywchang/Courses/PD/socpd-fig.pdf.
47. Ihe book: Frevert, R, Haase, J., Jancke, R., Knoechel, U., (Fraunhofer Institute for Integrated circuits, Dresden, Germany), and Kakerow, R., and Darianian, M., (Nokia research center, Bochum, Germany), "*Modeling and simulation for RF design*, Published by Springer P.O. Box 17, 3300 AA Dordrecht, The Nederlands, ISBN 10 0 -387-27584-3(HB), 2005.
48. In the paper: Streibl, M., Zängl, F., Esmark, K., Schwencker, R., Stadler, W., Gossner, H., Drüen, S., and Schmitt-Landsiedel, D., "*High abstraction level permutational ESD concept analysis*", Microelectronics Reliability, Vol. 45, 2005, pp. 313–321.
49. In the habilitation work: Hedrich, L., "*Entwurf integrierten analoger schaltungen mit Hilfe symbolischer Methoden*", Universitaet Hannover, Hannover, 2004.
50. In the report: Chalup, S.K., Mellor, D., and Rosamond, F., "*The Machine Intelligence Hex Project*", School of Electrical Engineering and Computer Science, the University of Newcastle, Australia, Technical Report, 21. June 2005. It is written: **„below we briefly outline the procedure, however anyone considering implementing this approach would be advised to consult a relevant book on circuit simulation, such as that by Litovski and Zwolinski (1997).”** http://www.cs.newcastle.edu.au/~chalup/papers/MIHex2005_tr.pdf.
51. In the book: Kahl, K., Edelkamp, K. and Hildebrand, L., "*Learning How to Play Hex*", Book Chapter in: J. Hertzberg, M. Beetz, and R. Englert (Eds.):*"KI 2007: Advances in Artificial Intelligence"*, LNAI 4667, ISBN 978-3-540-74564-8 pp. 382–396, 2007, Springer-Verlag Berlin Heidelberg
52. In the paper: Dong, W., Li, P., and Ye, X., "*WavePipe: Parallel Transient Simulation of Analog and Digital Circuits on Multi-Core Shared-Memory Machines*", 45th DAC, Anaheim, June 2008. http://www.dac.com/45th/PDFs/14.1_BEST_Paper.pdf,
53. In the chapter: McPherson, D.S. and Chrisostomidis, C.E., "*CAD techniques*", in the book: Robertson I.D., and Rocyszyn, S., "*RFIC and NINIC design and technology*", IEE Circuits,

devices, and systems series 13, IEE 2001. (First reference).

54. In the paper: Mistrı´k,P., Mullaley, C., Mammano, F., and Ashmore, J., "*Three-dimensional current flow in a large-scale model of the cochlea and the mechanism of amplification of sound*", J. of the Royal Socociety Interface, Vol. 32, No. 6, 2009, 279–291. It is written: **"To determine the pattern of current flow within the cochlear equivalent electrical circuit (figure 1*c*), we developed the solution techniques based on MNA (Litovski & Zwolinski 1997) and modified from SCAM (developed by E. Cheever; http://www.swarthmore.edu/NatSci /echeeve1/). MNA allows elements and their connectivities within a circuit of arbitrary complexity to be written down as a table and then to be mapped into a connectivity matrix."**
55. In the book: Lattarulo, F., "*Electromagnetic compatibility in power systems*", Elsevier, 2007, ISBN 0080452612, 9780080452616.
56. In the PhD thesis: Legrand, F., "*Modélisation de circuits électrotechniques en vue de leur simulation - Réalisation d'un simulateur*", L'Université Bordeaux I, École doctorale des sciences physiques et de l'ingénieur, 29 janvier 2004.
57. In the master theses: Subramanian, S., "*A Super nodal approach to the linear analog solver in a VHDL-AMS system*", The Division of Graduate Studies and Research Of The University Of Cincinnati, Department of Electrical and Computer Engineering and Computer Science of The College of Engineering, October 22nd 2003.
58. In the PhD thesis: Rasmussen, R.K., "*Algorithmic approach for playing and solving Shannon games*", The Faculty of Information Technology at The Queensland University of Technology, Brisbane, Australia, 2007.
59. In the Ph D Thesis: Kincl, E., "*Methods for testing of analog circuits*", Brno University of technology, Faculty of Electrical Engineering and Communication, Department of Radio Electronics, 2013.
60. In the master thesis: Frazier, N., "*Modeling frequency variations in ring oscillators with respect to process parameter variations*", The Graduate Faculty of Texas Tech. University, December 2002.
61. In the master thesis: Raghuram, R., "*Improving Simulation Time using Multithreading In Frequency Extended VHDL-*

		AMS", Master Thesis, Division of Graduate Studies and Research of the University of Cincinnati in the Department of Electrical and Computer Engineering and Computer Science of The College of Engineering, 2002. 62. In the book: Hurst, S. , "*VLSI Custom Microelectronics: Digital: Analog, and Mixed-Signal*", Publisher: CRC, Nov. 5, 1998, ISBN-10: 0824702204, ISBN-13: 978-0824702205 63. In the curriculum: *Course Information – 2009/2010, ECX5231- Network Theory*, Department of Electrical & Computer Engineering, Faculty of Engineering Technology, The Open University of Sri Lanka, Nawala, Nugegoda 10250. 64. In the book: Graeb, H., "*Analog Design Centering and Sizing*", Springer, 2007, ISBN 1402060033, 9781402060038 65. In the paper: Hsin-Hua Pan, Hung-Ming Chen, Chia-Yi Chang, "*Buffer/flip-flop block planning for power-integrity-driven floorplanning*," 10th Int. Symposium on Quality of Electronic Design, ISQED 2009, SAN JOSE, California, pp.488-493. 66. In the paper: Mistrik, P., and Ashmore, J., "*Using large scale computational model to study the effect of longitudinal and radial electrical coupling in the cochlea*", Proc. of the 10th Int. Workshop on the Mechanics of Hearing, Concepts And Challenges In The Biophysics Of Hearing, Keele University, Staffordshire, UK, 27 – 31 July 2008, edited by Nigel P Cooper (Keele University, UK) & David T Kemp (University College London, UK), pp. 377-383 67. In the PhD thesis: Ali, S.H.Md, "*System level performance and yield optimization for analog integrated circuits*", University of Southampton, Faculty of Engineering Science and Mathematics, School of Electronics and Computer Science, 2009. 68. In the paper: Chuang, Y.-L., , Lee, P.-W., and Chang, Y.-W., "*Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs*", Proceedings of the 2009 Int. Conf. on Computer-Aided Design, San Jose, California, 2009, ISBN:978-1-60558-800-1, pp. 666-673 and 69. In the paper: Hsu, Y.-C., Hsieh, M.F., McMahon, R.A., "*A General Design Method for Electric Machines Using Magnetic Circuit Model Considering the Flux Saturation Problem*", Proc. of the Eighth Int. Conf. on Power Electronics and Drive Systems, IEEE PEDS2009, November 2-5, 2009, Taipei,

		Taiwan, R.O.C, pp. 625-630 and 70. In the patent: Chen, H., "*S-Matrix technique for circuit simulation*", Pat. No. US 7,660,708 B2, 09 February, 2010. 71. In the PhD thesis: O'Neal, D. J., "*Cure Induced Stress Generation and Viscoelasticity in Polymer Coatings*", Faculty of the Graduate school of the University of Minnesota, January 2010. 72. In the master thesis: Krishnamachary, V., "*A Methodology for Analyzing VHDL-AMS Systems using an Experimental Design Approach*", Department of Electrical and Computer Engineering and Computer Science of The Coolege of Engineering, Division of Garaduate studies and research, University of Cincinnati, April 2002. 73. In the PhD thesis: Hsu, Y.-C., "*Design, Modeling and Validation of Permanent Magnet Generators for Wind Turbines*", Department of System and Naval Mechatronic Engineering, Taiwan, 2010. 74. In the paper: Streibl, M., et all., "*High Abstraction Level Permutatinal ESD Concept analysis*", Proceedings of the 2003 Electrical Overstress/ Electrostatic Discharge Symposium, Las Vegas, Nevada, USA, Sept. 200. pp. 2A.8.1-2A.8.9 75. In the master thesis: Rahman, A.B. A., "*Modelling of Mixed Physical-domain System*", University of Southampton, Faculty of Engineering, Science and Mathematics, School of Electronics and Computer Science, September 2010. http://eprints.soton.ac.uk/ 76. In the curriculum: "*Optimization based modeling and design of electronic circuits*", Professor Jose Ernesto Rayas Sanchez, from Instituto Tecnologico y de Estudios Superiores de Occidente, Gvadalajara, Mexico, 77. In the monograph: Francesco Lattarulo, F., *"Electromagnetic compatibility in power systems*", Elsevier Science, 2007, ISBN-10: 0080452612, ISBN-13: 978-0080452616, CHAPTER 9: Vergura, S., Liserre, M., and Vacca, F., "*Adjoint Network Theory to Analyse thePower Converters with Respect to their Line-side Behaviour*" 78. In the master thesis: Chandrashekar Chetput Lakshminarayanan, "*An Analog kernel using the direct method for solving ordinary differential algebraic equations in a Mixed_mode Simulator*", University of Cincinnati, Department of Electrical and Computer Engineering and Computer Science

		of The College of Engineering, December 1997 79. In the master thesis: Emanuel Dahlberg, "*Electricity in a 2D mechanics simulator for education*", Umeå University, Department of Computing Science, SE-901 87 UMEÅ, SWEDEN, January 31, 2011. 80. In the master thesis: Raghuram Srinivasan, "*Improving Simulation Time using Multithreading In Frequency Extended VHDL-AMS*", University of Cincinnati, Department of Electrical and Computer Engineering and Computer Science of The College of Engineering, 2002. 81. In the paper: Hsieh, M.; Hsu, Y.; "*A Generalized Magnetic Circuit Modeling Approach for Design of Surface Permanent Magnet Machines*", IEEE Transactions on Industrial Electronics, Vol. 59, No. 2, February 2012, pp. 779 – 792, ISSN: 0278-0046. 82. In the paper: Saibua, Siwat; Qian, Liuxi; Zhou, Di-an, "*Worst case analysis for evaluating VLSI circuit performance bounds using an optimization method* "**,** 2011 IEEE/IFIP 19th Int. Conf. on VLSI and System-on-Chip (VLSI-SoC), Kowloon, Hong Kong, Oct. 2011, pp. 102 – 105. E-ISBN: 978-1-4577-0169-6, Print ISBN: 978-1-4577-0171-9. 83. In the paper: Sasikanth Manipatruni, Dmitri E. Nikonov, and Ian A. Young, "*Circuit Theory for Analysis and Design of Spintronic Integrated Circuits*" (Condensed Matter > Mesoscale and Nanoscale Physics) http://arxiv.org/ftp/arxiv/papers/1112/1112.2746.pdf 84. In the report: Pande, S., Agrawal, S., Krishnamachary, V., Bapat, S., Balakrishnan, G., and Carter, H., "*Advanced Continuous-Time Methods for VHDL-AMS Mixed-Signal Simulation*", in the report: Dr. Harold W. Carter, Ed., "*Development, Exploitation, and Transition Of Computer Aided Engineering (CAE) Tools*", University of Cincinnati Dep. of Electrical and Computer Engineering and Computer Science, June 2003. 85. In the teaching notes: Kolka, Z., "*Počítačové řešení elektronických obvodů*", Faculty of Electrical Engineering and Communication, Brno University of Technology, 2010, http://www.umel.feec.vutbr.cz/VIT/images/pdf/skripta_VUT/Kolka_2010.pdf 86. In the Ph. D. thesis: Nechma, T.,"*Parallel Sparse Matrix Solution for Direct Circuit Simulation on a Multiple FPGA System*", University of Southampton Faculty of Physical And Applied Sciences, Electronics and Computer Science, 2012.

		87. In the paper: Sigala, R., Smerieri, A., Schüz, A., Camorani, P. and Erokhin, V., "*Modeling and simulating the adaptive electrical properties of stochastic polymeric 3D networks*", Modelling and Simulation in Materials Science and Engineering, Vol. 21, No. 7, (5007), doi:10.1088/0965-0393/21/7/075007, 2013 88. The company Hamster that claims it is the first independent producer of an VHDL-AMS simulator for personal computers, on the website http://www.hamster-ams.com/literature.htm, as a reference for modelling and simulation cites the book above. 89. In the project application: The University of Bordeaux, Department of informatics, "*Visualisation en Schematique Electrique*", as the first refernce cites the book above. http://www.dept-info.labri.u-bordeaux.fr/maylis/DEA/sujet. html. 90. In the paper: Melikian, V., "Logic *Simulation of Digital Circuits Exposed to Radiation*", Facta Universitatis, Series: Electronics and Energetics, Vol. 12, No.1, 1999, pp. 71-86, UDC 621.3.049.7. 91. In the paper: M Barke, M Kaergel, M Olbrich, "*Robustness measurement of integrated circuits and its adaptation to aging effects*", Microelectronics Reliability, Available online 12 February 2014, http://dx.doi.org/10.1016/j.microrel.2014.01.012 92. Zjajo,A., "*Stochastic Process Variation in Deep-Submicron CMOS Circuits and Algorithms*", 2014, DOI 10.1007/978-94-007-7781-1, Print ISBN 978-94-007-7780-4, Online ISBN 978-94-007-7781-1, Springer Netherlands. 93. In the Master thesis: Srinivasan Arunachalam, "*Quantum Speed-ups for Boolean Satisfiability and Derivative-Free Optimization*", University of Waterloo, Waterloo, Ontario, Canada, 2014. 94. In the PhD thesis: Jayanthy, S., "*Development of Algorithms for TestGeneration and Simulation of Crosstalk Delay Faults in VLSI Circuits*" for partial fulfilment for the award of the degree of Doctor of Philosophy Faculty of Electrical Engineering, Anna University Chennai 600 025, February 2012, http://hdl.handle.net/10603/23842. 95. Ajiboye, M. O, "*Synthesis of Analog Filter Using Evolutionary Strategies*", 2015, A Thesis Submitted to the Faculty of Graduate Studies Through the Department of Electrical and Computer Engineering in Partial Fulfillment of the Requirements for the Degree of Master of Applied Science at the University of Windsor, Windsor, Ontario, Canada,

http://scholar.uwindsor.ca/etd/5449.

96. R. Thomas, D.J.P. Lahaye, C. Vuik and L. Van Der Sluis, "*Transients in Power Systems: A Literature Survey*", Report 13-12, Delft University of Technology, ISSN 1389-6520, Reports of the Department of Applied Mathematical Analysis, Delft, 2013.
97. In the PhD thesis: Bousquet, L., "*Enriched high level model generation for heterogeneous and multiphysic systems*". Engineering Sciences. Université de Grenoble, 2014. French: Thèse pour obtenir le grade de Docteur De L'université De Grenoble. (In French)
98. Montgomery, R.D., "*Fractal Electrodes For Interfacing Neurons To Retinal Implants*", A Dissertation Presented to the Department of Physics and the Graduate School of the University of Oregon in partial ful€llment of the requirements for the degree of Doctor of Philosophy December 2014.
99. Bürger, J., Goudarzi, A., Stefanovic, D., Teuscher, C., "*Composing a Reservoir of Memristive Networks for Real-Time Computing*", arXiv 1504.02833 [cs.ET]. http://arxiv.org/pdf/1504.02833.pdf
100. Sowa, M., "*Application Of Stamps in the Automatic Formulation Of Circuit Equations – Part I. Basics*", ELEKTRYKA, No. 1, (225), Vol. LIX, 2013, pp. 43-52.
101. Bürger, J., Goudarzi, A., Stefanovic, D., and Teuscher, C., "*Computational Capacity and Energy Consumption of Complex Resistive Switch Networks*", arXiv: 1507.03716 [cs.ET], Vol. 3, Issue x, xxx–xxx page. DOI:10.3934/ms.2015.x.xxx, http://arxiv.org/pdf/1507. 03716.pdf
102. Bürger, J., Goudarzi, A., Stefanovic, D. and Teuscher, C., "*Hierarchical composition of memristive networks for real-time computing*", 2015 IEEE/ACM Int. Symp. on Nanoscale Architectures (NANOARCH), Boston, MA, July 2015, pp. 33 – 38, DOI: 10.1109/NANOARCH.2015.7180583.
103. Kolka, Z. , Biolkova, V., Wilfert, O., and Biolek, D., "*Simulation model of correlated FSO channels*", 2015 IEEE Conference on Microwave Techniques (COMITE), April 2015, pp. 1–4, Pardubice, Check Republic, DOI:10.1109/COMITE. 2015.7120328.
104. Ogrodzki, J., "*Analog approach to mixed analog-digital circuit simulation*", *Proc. SPIE* 8903, Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments 2013, 89031S, October 25, 2013,

doi:10.1117/12.2035235.
105. In the PhD thesis: Rasoulzadeh Darabad, M., "*A Fine-grained Approach to Parallelise the Circuit Simulation Process on Highly Parallel Systems*", A thesis for the degree of Doctor of Philosophy in the Faculty of Physical Sciences and Eng. Electronics and Computer Science, Uni. of Southampton, November 2015.
106. Y. Y. Chen, M. Gholipour, D. Chen, "*Flexible transition metal dichalcogenide field-effect transistors: A circuit-level simulation study of delay and power under bending, process variation, and scaling*" Proc. of the 21st Asia and South Pacific Design Automation Conf. (ASP-DAC) , Macau, 2016, pp. 761-768.
107. A Zjajo, "Brain-machine Interface, Circuits and Systems", Springer International Publishing Switzerland, 2016.
108. In the thesis: M. Alawein, "*Circuit Simulation of All-Spin Logic*" KAUST Repository, Program: Electrical eng., Dept. Computer, Electrical and Mathematical Sciences and Engineering (CEMSE) Division, King Abdullah Uni. of Science and Technology, May-2016.
109. In the Bachelor Thesis: Jurásek, L., "*Efficient LU factorization for sparse matrices*", ČVUT v Praze, (Czech Technical University in Prague. Computing and Information Centre) http://hdl.handle.net/10467/69618.
110. Kheirallah, R., "*Etude Statistique de l'Energie dans les Circuits Intégrés CMOS-FDSOI: Caractérisation et Optimisation*", Micro et nanotechnologies/Microélectronique, Uni. de Montpellier, France, Submitted on 8 Feb 2017, https://hal-lirmm.ccsd.cnrs.fr/tel-01462300.
111. Champac V., & Garcia Gervacio J., "*Gate Delay Under Process Variations*". In: "*Timing Performance of Nanometer Digital Circuits Under Process Variations*". Frontiers in Electronic Testing, vol 39. Springer, Cham. 2018.
112. Ying-Yu Chen, Morteza Gholipour & Deming Chen, "*Flexible transition metal dichalcogenide field-effect transistors: A circuit-level simulation study of delay and power under bending, process variation, and scaling*", 21st Asia and South Pacific Design Automation Conference (ASP-DAC), 25-28 Jan. 2016, DOI: 10.1109/ASPDAC.2016.7428103, Publisher: IEEE, Macau, China.
113. Liang, J., "*An Improvement on Extended Impedance Method*

		towards Efficient Steady-State Analysis of High-Frequency Class-E Resonant Inverters", Published in: 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), 20-24 May 2018, DOI: 10.23919/IPEC.2018.8507467, IEEE, Niigata, Japan. 114. Melikyan V., "*General Issues of Gate-Level Simulation and Optimization of Digital Circuits with Consideration of Destabilizing Factors*". In: Simulation and Optimization of Digital Circuits. Springer, Cham, 2018. 115. Jayanthy S., Bhuvaneswari M.C., "*Simulation of Asynchronous Sequential Circuits Using Fuzzy Delay Model for Crosstalk Delay Faults*". In: Test Generation of Crosstalk Delay Faults in VLSI Circuits. Springer, Singapore, 2019. 116. Erokhin V. "*3D Systems with Stochastic Architecture*". In: *Fundamentals of Organic Neuromorphic Systems*. Springer, Cham. 2022, https://doi.org/10.1007/978-3-030-79492-7_7 117. In the MS thesis: Mackenzie Wootton, "Experimental Analysis of Electric Double Layer and Lithium-Ion Capacitors for Energy Storage Systems and Their Application in a Simulated DC Metro Railway System", McMaster University (Electrical & Computer Engineering) Hamilton, Ontario, Canada, 2018. 118. Greg Poole, "*Electrical Schematic of The Earth And Solar System*", Fundamental Journal of Modern Physics ISSN: 2249-9768, Vol. 13, No. 2, 2020, Pages 121-139. 119.
C	**6**	The book: (**9.15**) V. Litovski, S. Lazović. "*Basic Electronics*", in Serbian, Čuperak Plavi, Niš, 1996, was cited: 1. In the paper: Priem, F., Calu, J. and de Craemer, R., "*Towards the integration of course modules of different european institutions of higher education into a multimedia learning platform*", Annual Journal of Electronics, 2009, ISSN 1313-1842, 2. In the paper: Petrovic, V., Ilic, M., Schoof, G., Stamenkovic, Z., "*Integrated Single Event Latchup protection for ASICs used in space applications*", 21st Telecommunications Forum (TELFOR), Nov. 2013, DOI: 10.1109/TELFOR.2013.6716308**,** Belgrade, Serbia. 3. In the paper: Karoussos, E., Pavlović, V.D., "A novel high-performance complete fully differential two-stage cascade

		amplifier in bipolar transistor implementation", Scientific Publications of the State University of Novi Pazar Series A: Applied Mathematics, Informatics and mechanics 2012, Vol. 4, No. 1, str. 25-37. 4. *In the paper: Ružica, S., "*Tiristorsko usmeravanje sa uglom protoka manjim od 90 stepeni*", Tehnika – Elektrotehnika, 2008, vol. 57, br. 5, str. 9-13. 5. In the PhD thesis: Petrovic, V., "*Design Methodology for highly Reliable Digital ASIC Designs Applied to Network - Centric System Middleware Switch Processor*", Von der Fakultät für Mathematik, Naturwissenschaften und Informatik der Brandenburgischen Technischen Universität Cottbus-Senftenberg, Germany. 6. *In the paper: Janjić, I., "*Mikrokontrolerska realizacija ordinarnog delta modema za prenos govornog signala*", INFOTEH-JAHORINA Vol. 13, March 2014, pp. 1146-1150.
Ci	**1**	The book: (**9.17**) Litovski V., Milovanović D., Petković P., Milenković S., Randjelović Z., Panić V., Ilić T., *"*Zbornik rešenih zadataka iz osnova elektronike*", (in Serbian), was cited: 1. *In the curriculum: Софтић, Ф., „*Електротехнички материјали и компоненте*", Електротехнички факултет Бања Лука, http:// www.etfbl.net/?c=prikazi&objekat=sadrzaj&f_id=4383&ss_jezik=1
Cii	**2**	The book: (**9.18**) V.B. Litovski: CAD of electronic circuits, DIGP "Nova Jugoslavija", Vranje, 2000 (in Serbian) is cited in 1. Che Bin, Fan Xiaoya**,** "Testability Design for SoC Based on IDDQ Scanning", Computer Measurement & Control, Vol. 17, No. 8, 2009. 2. Barac, D., "*A contribution to testing of fiscal memories*", 19th Telecommunications Forum (TELFOR),Nov. 2011, **DOI:** 10.1109/TELFOR.2011.6143689 Belgrade, Serbia.
Ciii	**6**	The book: (**9.21**) Litovski, V., *"Osonovi elektronike, Teorija rešeni zadaci i ispitna pitanja"*, Akademska Misao, Beograd, 2006. god., was cited: 1. University of Rostock, Germany, Department of Micro-electronics & CE, within: *Project: Integrated Circuit Design 1, Task:* Power Operation Amplifier, *Technology:* CMOS-Technology, *Mentor: Prof. Dr. Beikirch, Student:* Dejan Vidanovic, Matri. No. – 4299525, http://users.verat.net/~simeone/Project Integrated Circuit Design 1.pdf. 2. In the curriculum: Софтић, Ф.,* „*Електротехнички*

		материјали и компоненте“, Електротехнички факултет Бања Лука, http://www.etfbl.net/?c=prikazi&objekat=sadrzaj&f_id=4383&ss_jezik=1 3. In the papr: Petrovic, V., Ilic, M.,Schoof, G.,Stamenkovic, Z., "*Integrated Single Event Latchup protection for ASICs used in space applications*", 21st Telecommunications Forum (TELFOR), Nov. 2013, pp. 624 - 627, Print ISBN: 978-1-4799-1419-7 4. In the paper: Karoussos E., and Pavlović V.D., "*A novel high-performance complete fully differential two-stage cascade amplifier in bipolar transistor implementation*", Scientific Publications of the State University of Novi Pazar Series A: Applied Mathematics, Informatics, and Mechanics, 2012, vol. 4, br. 1, str. 25-37. 5. *In the paper: Janjić, I., "*Mikrokontrolerska realizacija ordinarnog delta modema za prenos govornog signala*", Proc. of Infoteh-Jahorina, Vol. 13, March 2014 , pp. 1146-1150. 6. In the Dissertation: Petrovic, V., *"Design Methodology for highly Reliable Digital ASIC Designs Applied to Network-Centric System Middleware Switch Processor"*, Von der Fakultät für Mathematik, Naturwissenschaften und Informatik der Brandenburgischen Technischen Universität Cottbus - September, 2013.
	528	

4. Engineering engagement

The main research subject of Prof. Litovski’s, computer aided design of electronic circuits, was chosen thanks to the iniciative of “Elektronska industrija” and the Ministry (in those times Community) of Science of Serbia in the year 1978. Since then, being supported by Elektronske industrije, The Regional Community of Science in Niš, The Serbian Ministry of Science, The Serbian Council for internatonal scientific collaboration, the Yugoslav peoples army, and the Fcaulty of Electronic Engineering in Niš, a line of successful research may be followed. For example, in the year 1997, only two years after the lift of the international sanctions against Yugoslavia, in, under the leadership of Prof. Litovski three integrated circuits were designed and samples produced. While not explicitly pronounced, all three chips were intended to be built in domestic products. One should consider these results as an important contribution to the regeneration of this kind of knowledge in Serbia after the lifting of the sanctions.

To the name of Prof. Litovski is connected the design of the first Serbian custom integrated circuit in the year 1990, that was designed in collaboration of "Ei Mikroelektronika" from Niš, "Rudi Čajavec" from Banja Luka and the Faculty of Electronic Engineering in Niš. It was completely produced in Serbia including the silicon cristal. Similarly, the first mixed-signal integrated circuit in Serbia was designed in LEDA in collaboration with the Middlesex University from London, Englandin the year 1992.

The private consultant William Lurie, from Bocca Raton-a (21061 Cottonwood Drive), Florida 33428, USA, in the early eighties of the past century, developed and produced electrical telecommunication filters based on the published designs of Prof. Litovski.

Prof Litovski was leading several research and educational project financed by the Yugoslav and Serbian Governement and by several European authorities. Following is the list of project in reverse time order:

Financed by domestic resources

2011- …"Advanced technologies for measurement, control, and communication on the electric grid"

2004-2007 "A system for power factor measurement and correction of electronic equipment", funded by the Ministry of Science of Serbia (code 232014).

2002-2004 "Design testing and eco-design of electronic circuits and systems" funded by the Ministry of Science of Serbia (code IT.1.02.0075.A).

1996-2000 "Integrated Circuit Design Automation". Funded by the Ministry of Science of Serbia

1994-1996 "Complex Microelectronic Devices Design". Funded by the Ministry of Science of Serbia

1991-1995 "Development of System for IC Design and Verification" funded by the Ministry of Science of Serbia.

1991-1994 "Software development for design automation of Application specific CMOS integrated circuits", funded by Yugoslav Faderal Ministry of Science.

1986-1990 "Semiconductor Microelectronics and Optoelectronics" funded by the Ministry of Science of Serbia

1981-1985 "Microelectronics Devices" funded by the Ministry of Science of Serbia

Financed by foreign resources

2015-2016 The SYNAPS project, Realized by the Dept. of Electronics and Electrical Eng. at the University of Bath, UK, Project code RE-EE1107.

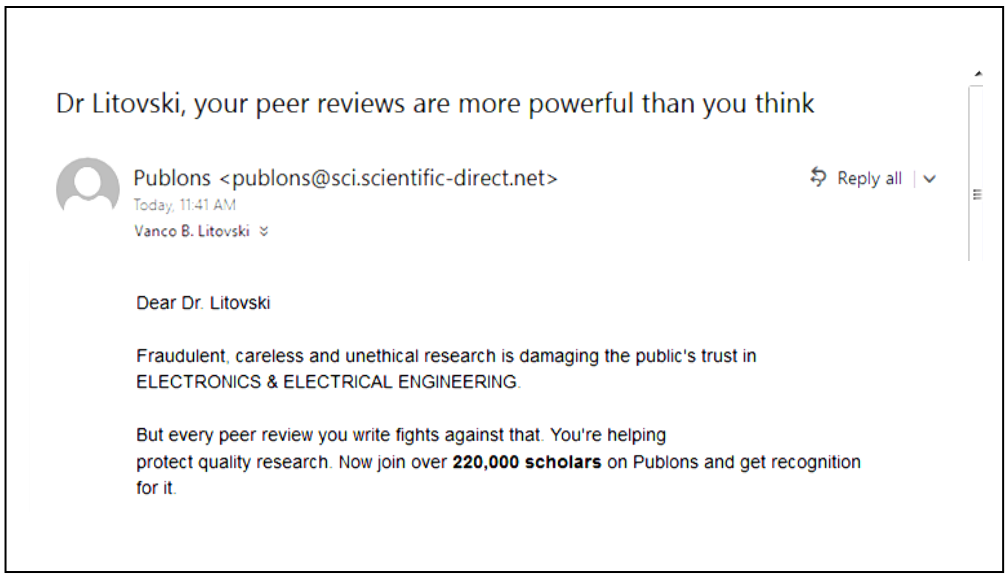
2010-2011 The ISSNBS project, Realized within the Pact of Stability of Southeast Europe and funded by The German Government (DAAD).

2008-2010 "South-Eastern European GRID eInfrastructure for regional eScience-SEE-GRID-SCI" Specific Support Action SEE-GREID-SCI, Funded by the Commission of the European Community, Infromation Society and media Directorate-General.
2006-2008 "South-Eastern European Grid-Enabled eInfrastructure Development 2" Specific Support Action SEE-GREID-2, Funded by the Commission of the European Community, Infromation Society and media Directorate-General.
2007-2008 "System on Chip design**",** funded by TEMPUS JEP-41107-2006
2001-2007 ISSNB, Realized within the Pact of Stability of Southeast Europe and funded by The German Government (DAAD).
2005-2007 "Electronic education in Serbia", TEMPUS CD_JEP.17028.2002.
2005-2007 "Course Development Program +", which is being implemented by WUS Austria within its program "Support to Higher Education in Bosnia and Herzegovina in 2005/ 2007" (No: 7967-00/2005)
2000-2002 Researcher on a set of small projects with Middlesex University, London ("Low bit High Speed BOSA DSM", "Evaluation and Design of a High Frequency Low Pass Oversampling DAC" i "Band Pasas Oversampling AD Converter".)
1999-2000 Research project realized with the University of Southampton funded by the British EPSRC (Grant no. GR/M85531, 02 July 1999).
1995-1995 A research project realized with the University of Southampton funded by the British EPSRC. (Grant ref. No. GR/K54129, 12 June 2005).
1989-1991 A research project realized with the University of Southampton funded by the British Council (Alis No. 245, Belgrade).

4.a Other professional activities

1. Senior member of the "Serbian Academy of Engineering Sciences", Belgrade
2. Founder and the first president of Yugoslav Simulation Society.
3. Member of IEEE.
4. Member of the presidency of ETRAN
5. President of the Organizing Committee of the Small Systems Simulation Symposium held at the University of Niš.
6. Editor of the Proceedings of the "Small Systems Simulation Symposium"
7. Founder and first editor of the journal "Facta Universitatis, Series: Electronics and Energetics" published by the University of Niš.
8. Currently : Representative of Serbia at the PAB (Public Authority Board) of the Joint Undertaking ARTEMIS with the EC Commission

9. Currently: President of the Coordinating Council for ICT at the regional Chamber of Commerce in Niš.
10. Member of Edtorial Board: The Journal Electronics;
11. Member of the stearing committees of: Conf. TELSIKS, MIEL, INDEL, SSSS, NEUREL.
12. As an expert, by appointment No. AL00065673, of the EC (Information Society and Media / Embedded Systems and Control) I am currently reviewer of the Moby-Dic scientific project (No. 248858) financed within the FP7.
13. President of the Board of the Nis Cluster of Advanced Technologies - NiCAT
14. Reviewer for: IEEE CAS; IEEE TCAD II; Microelectronics Reliability; IEE Proceedings; IEEE CAD of ICAS; Int. J. of Electronics; J. of Circuits Systems and Computers; Int. J. of Information technology; Serbian J. of Electrical Engineering; COMPEL; IEEE ISCAS (symp.); ETRAN (Conf.); IASTED (Conf).; TELFOR (Conf.); TELSIKS (Conf.); SSSS (Conf.), AFRICON 2013 (Conf.), ICT Innovation 2013 (Conf.), ICMRA 2013 (Conf.), PEMC 2014, (Int. power electronics and motion control Conf. and exhibition), IEEE Access.


Dr Litovski, your peer reviews are more powerful than you think

Publons <publons@sci.scientific-direct.net>
Today, 11:41 AM
Vanco B. Litovski

Reply all

Dear Dr. Litovski

Fraudulent, careless and unethical research is damaging the public's trust in ELECTRONICS & ELECTRICAL ENGINEERING.

But every peer review you write fights against that. You're helping protect quality research. Now join over **220,000 scholars** on Publons and get recognition for it.

15. Guest editor of the „Electronics ISSN 1450-5843“, Vol. 16, No. 1, June 2012.

4.b Awards

- The Savastano Award for 1998 (Federation of the European Simulation Societies)
- The Tesla Award for 1994 (The Tesla Foundation)
- The ETRAN Award for 1986 (The Association for ETRAN)
- A long list of recognitions by the Faculty of Electronic Engineering, University of Niš, The Town of Niš, The University of Banja Luka, and the University of Eastern Sarajevo.

5. LIST OF PUBLICATIONS (Papers written in Serbian are marked by an asterix)

5.a Monographs

a.1.* **Litovski, V.**, *"Automatizacija projektovanja integrisanih kola"*, u "MIPRO'88 Mikroelektronički sklopovi-principi rada i projektiranja", pod redakcijom prof. Petra Biljanovića, Rijeka, Maj, 1988. (Serbian)

a.2.* **Litovski, V.**, *"Logička simulacija"*, u monografiji: "Projektovanje VLSI, I deo", Nauka, Beograd, 1991, pp. 106-181.

a.3.* Radenković,T., Radenković, Z., **Litovski, V.**, *"Integrisani softverski paket za projektovanje gejtovskih matrica (ISPGM)"*, u monografiji "Projektovanje VLSI, I deo", Nauka, Beograd, 1991, pp. 411-481. (Serbian)

a.4. Andrejević Stošović, M., **Litovski, V.**, ***"****ANN Application to Modelling of the D/A and A/D Interface for Mixed-Mode Behavioural Simulation"***,** Micro Electronic and Mechanical Systems, Edited by Kenichi Takahata, Intech, ISBN 978-953-307-027-8, 2009, pp. 369-384.

Your Chapter has reached 10000 downloads
Miona Andrejevic Stosovic
Actions
To:
Vanco B. Litovski
Attachments:
InTech-Article_Stats.pdf (124 KB) [Open as Web Page]

Monday, March 23, 2015 8:17 AM

Od: InTech Author Stats [authorstats@intechopen.com]
Poslato: 23. mart 2015 0:37
Za: Miona Andrejevic Stosovic
Tema: Your Chapter has reached 10000 downloads

Dear Prof. Andrejević Stošović,

We are pleased to inform you that your paper "Electronic Circuits Diagnosis Using Artificial Neural Networks" has achieved impressive readership results. The chapter you have published with InTech in the book "Micro Electronic and Mechanical Systems" has so far been accessed 10000 times. Congratulations on

the significant impact that your work has achieved to date.

The top downloads of your paper are from the following five countries:
United States of America
India
China
United Kingdom
Japan

More information and statistics regarding your paper can be found on your Author Panel:
http://www.intechopen.com/account/login

---

a.5. Andrejević Stošović, M., **Litovski, V.**, ***"****Electronic Circuits Diagnosis Using Artificial Neural Networks"****,*** Micro Electronic and Mechanical Systems, Edited by Kenichi Takahata, Intech, ISBN 978-953-307-027-8, 2009, pp. 385-404.

a.6. Milić, M., **Litovski, V.**, ***"****New concepts of asynchronous circuits worst-case delay and yield estimation"****,*** Micro Electronic and Mechanical Systems, Edited by Kenichi Takahata, Intech, ISBN 978-953-307-027, 2009, pp. 455-476.

a.7. Litovski, V. B., „Electronic Filters, Theory, Numerical receipts, and design practice based on the RM software", Springer, 2019, ISBN 978-981-329-851-4.

b. Invited papers published in international journals

b.1. Damnjanović, M., **Litovski, V.**, *"A Survey of Routing Algorithms in Custom IC Design"*, J. of Semicustom ICs, (ISSN 0026-2692, Microelectronics Journal (Incorporating Journal Of Semicustom Ics)), Vol. 7, No.2, December, 1989, pp. 10-19.

c. Paper published in international journals

c.1. Raković, B.D., **Litovski, V.**, *"Least-Squares Monotonic Lowpass Filters with Sharp Cutoff"*, Electronic Letters, ISSN: 0013-5194, Vol. 9, No. 4, 1973, pp. 75-76.

c.2. Raković, B.D., **Litovski, V.**, *"Monotonic Passband Low-Pass Filter With Chebyshev Stopband Attenuation"*, IEEE Trans.on Acoustics, speech, and signal processing, ISSN**:** 0096-3518, Vol. ASSP-22, 1974, pp. 39-44.

c. 3. **Litovski, V.**, Raković, B.D., *"Attenuation Characteristics and Element Values of Least-Squares Monotonic Passband Filters With an Arbitrary Number of Transmission Zeros"*, Publications of Electrical Engineering Faculty, Uni. Belgrade, Series Electronics, Telecommunications and Automation (ETA), No. 97-101, 1974, pp. 67-101.

c.4. **Litovski, V.**, Lazović, S., *"Design of General Stopband Lowpass Filters with Equiripple Passband Response"*, Publikacije Elektrotehničkog fakulteta, Serija ETA, No. 102-106, 1974, pp. 45-52.

c.5. **Litovski, V.**, *"Synthesis Of Monotonic Passband Sharp Cutoff Filters With Constant Group Delay Response"*, IEEE Trans. on Circuits and Systems, ISSN: 1549-8328, Vol. CAS-26, No. 8, 1979, pp. 597-602.

c.6. **Litovski, V.**, Milovanović, D., *"New Solution For The Ideal Filter Approximation Problem"*, IEE Proceedings, Pt. G. , ISSN, 0143-7089,Vol. 130, No. 4, August, 1983, pp. 161-163.

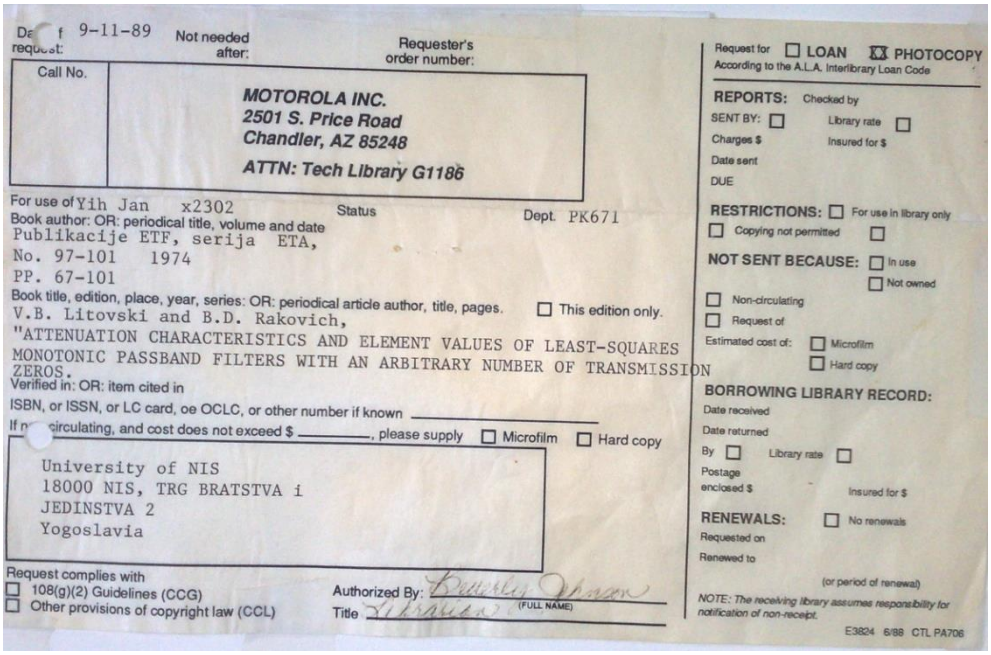
c.7. Glozić, D., **Litovski, V.**, Bayford, R., *"ASCOTA3 - A New Automatic Hierarchical CMOS Opamp Synthesizer"*, Facta Universitatis, series: Electronics and Energetics, Vol. 4, No. 1, 1991, pp. 81-105.

c.8. Milovanović, D., **Litovski, V.**, *"Fault Models Of CMOS Transmission Gate"*, Int. J. of Electronics, ISSN 0020-7217, Vol. 71, No. 4, May, 1991, pp. 675-683.

c.9. Radenković, Z., Radenković, T., Stojilković, S.M., **Litovski, V.**, *"A Knowledge - Based Layout Compaction Procedure"*, Microelectronics Journal, Vol. 23, No. 2, April, 1992, pp. 121-132.

c.10. **Litovski, V.**, Rađenović, J., Mrčarica, Ž., Milenković, S., *"MOS Transistor Modelling Using Neural Network"*, Electronics Letters, Vol. 28, No. 18, Avgust, 1992, pp. 1766-1768.

c.11. Mrčarica, Ž., **Litovski, V.**, *"A New Ideal Switch Model For Time-Domain Circuit Analysis"*, Int. J. of Electronics, ISSN 0020-7217, Vol. 74, No. 2, 1993, pp. 241-250.



Date of request: 9-11-89 Not needed after: Requester's order number:

Call No.

MOTOROLA INC.
2501 S. Price Road
Chandler, AZ 85248
ATTN: Tech Library G1186

For use of Yih Jan x2302 Status Dept. PK671

Book author: OR: periodical title, volume and date
Publikacije ETF, serija ETA,
No. 97-101 1974
PP. 67-101

Book title, edition, place, year, series: OR: periodical article author, title, pages. ☐ This edition only.
V.B. Litovski and B.D. Rakovich,
"ATTENUATION CHARACTERISTICS AND ELEMENT VALUES OF LEAST-SQUARES MONOTONIC PASSBAND FILTERS WITH AN ARBITRARY NUMBER OF TRANSMISSION ZEROS.
Verified in: OR: item cited in

ISBN, or ISSN, or LC card, oe OCLC, or other number if known

If not circulating, and cost does not exceed $ _____, please supply ☐ Microfilm ☐ Hard copy

University of NIS
18000 NIS, TRG BRATSTVA i
JEDINSTVA 2
Yogoslavia

Request complies with
☐ 108(g)(2) Guidelines (CCG)
☐ Other provisions of copyright law (CCL)

Authorized By: Beverly Inman (FULL NAME)
Title Librarian

Request for ☐ LOAN ☒ PHOTOCOPY
According to the A.L.A. Interlibrary Loan Code

REPORTS: Checked by
SENT BY: ☐ Library rate ☐
Charges $ Insured for $
Date sent
DUE

RESTRICTIONS: ☐ For use in library only
☐ Copying not permitted ☐

NOT SENT BECAUSE: ☐ In use ☐ Not owned
☐ Non-circulating
☐ Request of
Estimated cost of: ☐ Microfilm ☐ Hard copy

BORROWING LIBRARY RECORD:
Date received
Date returned
By ☐ Library rate ☐
Postage enclosed $ Insured for $

RENEWALS: ☐ No renewals
Requested on
Renewed to
(or period of renewal)

NOTE: The receiving library assumes responsibility for notification of non-receipt.

E3824 6/88 CTL PA706

c.12. Petković, P., **Litovski, V.**, *"New Generalized Approach to the Macromodeling of Digital Structures"*, Electron Technology, Vol. 26, No. 2/3, Warsaw, Poland, 1993, pp. 53-75.

c.13. **Litovski, V.**, Mrčarica, Ž., *"Macromodeling With Spice's Nonlinear Controlled Sources"*, IEEE Circuits and Devices Magazine, Vol. 9, No. 6, November, 1993, pp. 14-17,51.

c.14. Milovanović, D., **Litovski, V.**, *"Fault Models Of CMOS Circuits"*, Microelectronics and Reliability, Vol. 34, No. 5, May, 1994, pp. 883-896.

c.15. Glozić, D., **Litovski, V.**, Bayford, R., *"ASCOTA3 ADIL: A New Reconfigurable CMOS Analogue VLSI Design Framework"*, Microelectronics Journal, Vol. 25, No. 5, Aug., 1994, pp. 335-351.

c.16. Milenković, S., **Litovski, V.**, *"New Analytical Procedure For Automatic Cell Placement In Gate-Arrays"*, IEE Proceedings part G, Circuits Devices System, Vol. 141, No. 6, Dec., 1994, pp. 476-482.

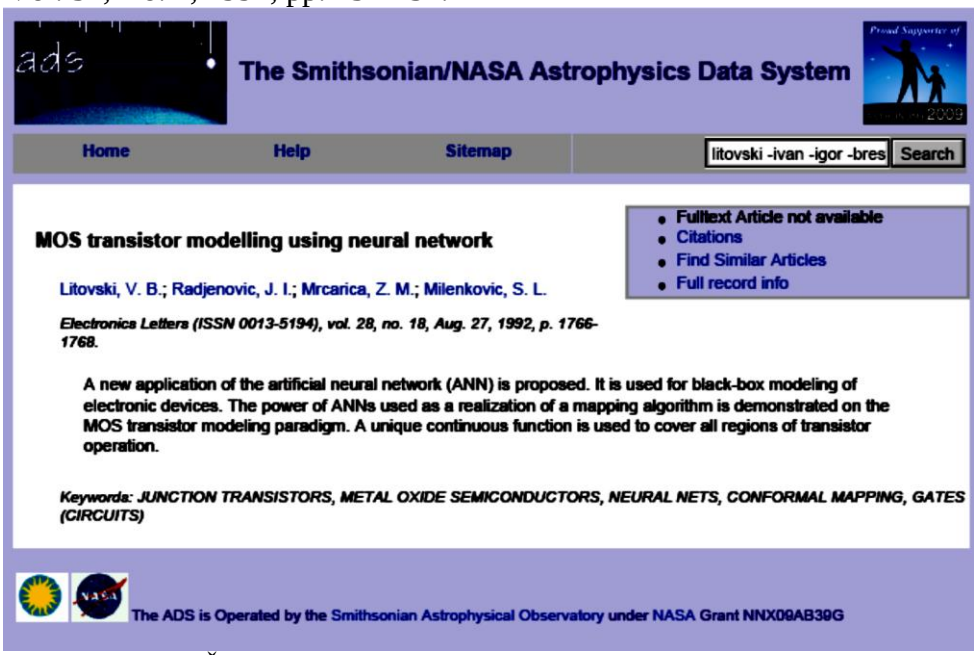
c.17. Petković, P., Stojilković, S., **Litovski, V.**, "*New Factorization Algorithm For Symbolic Circuit Analysis*", Electronic Letters, Vol. 31, No. 13, 22. Jun, 1995, pp. 1026-1027.

c.18. Mrčarica, Ž., Vujanić, A., Detter, H., **Litovski, V.**, "*Simulation Of Micromechanical Systems*", 6th Int. J. of Theoretical Electrotechnics, Thessaloniki, Greece, Sep., 1996, pp. 141-148.

c.19. Rađenović-Mrčarica, J., Mrčarica, Ž., Detter, H., **Litovski, V.**, *"Neural Network Visual Recognition For Automation Of The Microelectromechanical Systems Assembly"*, Int. J. on Neural Systems, Vol.

8, No. 1, Feb., 1997, pp. 69-79.

c.20. Petković, P., Milovanović, D., **Litovski, V.**, *"Symbolic Fault Modelling And Test Generation Of MOS Circuits"*, Microelectronics and Reliability, Vol. 37, No. 1, 1997, pp. 137-157.



c.21. Mrčarica, Ž., **Litovski, V.**, Detter, H., *"Modelling And Simulation of Microsystems Using Hardware Description Language"*, Research J. on Microsystem Technologies, Vol. 3, No. 2, Feb., 1997, pp. 80-85.

c.22. **Litovski, V.**, Mrčarica, Ž., Ilić, T., *"Simulation of Non-Linear Magnetic Circuits Modelled Using Artificial Neural Network"*, J. Simulation Practice and Theory, ISSN: 1569-190X, Vol. 5, No. 6, 1997, pp. 553-570.

c.23. Maksimović, D., **Litovski, V.**, *"Logic Simulation Based Method For Digital CMOS VLSI Circuits Power Estimation "*, 7th Int. J. Of Theoretical Electrotechnics, Join to ISTET '97, Cottbus, 1999, pp. 40-43.

c.24. **Litovski, V.**, Dimić, Ž., Damnjanović, M., Mrčarica*, Ž., "Electronic Circuit Simulatoion in a Mixed-Language Environment*", Microelectronics Journal, Vol. 29, No. 8, 1998, pp. 553-558.

c.25. Maksimović, D., **Litovski, V.**, "*Tuning Logic Simulators for Timing Analysis*", Electronics Letters, Vol. 35, No. 10, 13th May, 1999, pp. 800-802.

c.26. Mrčarica, Ž., Ilić, T., **Litovski, V.**, "*Time-Domain Analysis of Nolinear Switched Networks With Internally Controlled Switches*", IEEE Transactions on Circuits and Systems I, ISSN: 1057-7122, Vol. 46, No. 3,

March, 1999, pp. 373-378.
c.27. Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., **Litovski, V.**, "*Transient Electro-Thermal Simulation Of Microsystems With Space-Continuous Thermal Models In Analogue Behavioural Simulator*", Microelectronics and Reliability, Vol. 40, No. 3, March 2000, pp. 507-516.
c.28. Ilić, T., **Litovski, V.,** Litovski, I., Stojilković, S., "*Computationally Efficient Large-Change Statical Analysis of Linear Electronic Circuits*", Microelectronics and Reliability, Vol. 40, 2000, pp. 1023-38.
c.29. **Litovski, V.,** Maksimović, D., and Mrčarica, Ž., "*Mixed-signal modelling with AleC++: Specific features of the HDL*", Simulation Practice and Theory, ISSN: 1569-190X, Vol. 8, 2001, pp. 433-449.
c.30. Jakovljevic M., Fotiu P.A., Mrčarica Ž., **Litovski V.** and Detter H., "*Electro-thermal simulation of microsystems with mixed abstraction modelling* " Microelectronics Reliability, Volume 41, Number 6, June 2001 , pp. 823-835(13), Elsevier.
c.31. Damnjanović, M., Anđelković, B., **Litovski**, V., "*VHDL-AMS Compiler for Alecsis Simulation Environment*", Electronics, Vol. 6, No. 2, December 2002, pp. 6-11.
c.32. Stefanović, D., Kayal, M., **Litovski**, V.B., "*An Interactive Knowledge Based Analog Design Approach*", Electronics, Vol. 6, No. 2, December 2002, pp. 22-25.
c.33. Janković, S., Maksimović, D., **Litovski**, **V.B.**, "*Modern 32-bit Microcontroller Characteristics and Automotive Applications*", Electronics, Vol. 6, No. 2, December 2002, pp. 62-76.
c.34. Milojković, J., **Litovski, V. B.,** "*Eco-Design in Electronics – The State of the Art*", Facta Universitatis, Series: Working and Living Environmental Protection, Vol. 2, No. 2, 2002, pp. 87-100.
c.35. **Litovski, V.**, "*New Methods in Modeling and Simulation of Electronic Circuits and Systems*", Scientific Review, No. 29-30, 2001-2002, pp.189-207.
c.36. Maksimović, D., **Litovski, V.**, "*Logic simulation methods for longest path delay estimation*", IEE Proceedings Computers and Digital Techniques, Vol. 149, No. 2, 2002, pp. 53-59.
c.37. Savić, M., **Litovski, V.,** "*Behavioral object-oriented frequency domain electronic simulation*", Simulation News Europe, No. 38/39, December 2003, pp. 38-39.
c.38. Andrejević, M., **Litovski, V.,** "*Electronic Modelling Using Artificial neural networks* ", J. of Automatic Control, University of Belgrade, Vol. 13, No. 1, 2003, pp. 31-37.
c.39. **Litovski, V. B.**, Andrejević, M., Petković, P., Damper, R., "*ANN Application to Modeling of the D/A and A/D Interface for Mixed-Mode*

Behavioural Simulation", J. of Circuits, Systems and Computers, Vol. 13, No. 1, February 2004, pp. 181-192.

c.40. **Litovski,V.,** Litovski, I., and Zwolinski, M., "*Concurrent analogue fault simulation, the equation formulation aspect*", Int. J. of Circuit Theory and Aplications, Vol. 32, December 2004, pp. 467-507.

c.41. Andrejević, M., **Litovski, V.,** and Zwolinski, M., "*Black-Box Application in Modeling of Micro-electro-mechanical Systems*", Electronics, Vol. 8, No. 2, December 2004, pp. 27-30.

c.42. Dimitrijević, M., and **Litovski, V**., "*Implementation of the component characteristic curve tracer using PC-based acquisition card*", Electronics, Vol. 8, No. 2, December 2004, pp. 35-38.

c.43. **Litovski, V**., Andrejević, M., and Zwolinski, M., "*Acceleration of MEMS fault simulation using ANNs*", Electronics, Vol. 8, No. 2, December 2004, pp. 49-53.

c.44. Milenković, S., and **Litovski, V.**, "*Passive image rejection filters optimized for telecommunication application*", Electronics, Vol. 8, No. 2, December 2004, pp. 54-63.

c.45. Savić, M., and **Litovski, V.,** "*Bandgap voltage reference in CMOS*", Electronics, Vol. 8, No. 2, December 2004, pp. 68-70.

c.46. Savić, M., Mrčarica, Ž., and **Litovski, V.**, "*Ideal Switch Model Speeds Up the Switched Circuits Simulation*", WSEAS Transactions on Circuits and Systems, Vol. 4, No. 11, November 2005, pp. 1657-1663.

c.47. Savić, M. and **Litovski, V.**, "*Comparison of ideal and SPICE switches for electronic circuit simulation*", Simulation News Europe, Issue 43, July 2005, pp. 17-19.

c.48. Savić, M. **Litovski, V.**, and Mrčarica, Ž., "*Electronic circuit simulation with ideal switches*", HAIT J. of Science and Engineering, B 2, No. 3-4, 2005, pp. 476-495.

c.49. Milojković, J., and **Litovski, V.**, "*Concepts of computer take-back for sustainable end-of-life*", Facta Universitatis, Series: Working and Living Environmental Protection, Vol. 2, No. 5, 2005, pp. 363-372.

c.50 Sokolović, M., Savić, M., Nikolić, M., Litovski, V., Jevtić, M., and Petković, P., "*Testing and Diagnostic of ADC and Integrated Powermeter*", Electronics, Vol. 9, No. 1, 2005, ISSN 1450-5843.

c.51. **Litovski, V.,** Andrejević, M., and Zwolinski, M. "*Analogue electronic circuit diagnosis based on ANNs* ", Microelectronics Reliability, Vol. 46, No. 8, 2006, pp. 1382-1391.

c.52. **Litovski, V**., Savić, M., and Mrčarica, Ž., "*Ideal Switch Model Cuts Significantly Simulation Time*", IEEE Circuits and Devices Magazine, ISSN: 8755-3996, Vol. 22, No. 4, July/August 2006, pp. 16-22.

c.53. Milojković, J., and **Litovski, V.,** „*Take back concepts and end-of-life*

management of power electrical components“, Electronics, Vol. 10, No. 2, December 2006, pp. 59-63. YU ISSN 1450-5843

c.54. Anđelković, B., **Litovski, V.,** and Zerbe, V., “*Mission Level Modeling And Simulation Language For Mixed-Signal System-On-A-Chip Design*", J. of Circuits, Systems and Computers (World Scientific Publishing Company), Vol. 16, No. 1, February 2007, pp. 15-28.

c.55. Anđelković, B., and **Litovski, V.,** „*Parallel transistor level simulation based on parallel equation formulation implementated on Beowulf cluster*“, Simulation News Europe, Vol. 17, No. 3/4, December 2007, pp. 55-58. ISSN 0929-2268.

c.56. Dimitrijević, M., and **Litovski, V.B**., „*Implementation of compact switching power supply with high power factor*“, Electronics, Vol. 11, No. 1-2, December 2007. ISSN 1450-5843.

c.57. Sokolović, M., **Litovski, V.,** Zwolinski, M., “*New Concepts of Worst Case Delay and Yield Estimation in Asynchronous VLSI Circuits***”,** Microelectronics Reliability, ISSN 0026-2714, February, 2009, Vol. 49, No. 2, pp. 186-198.

c.58. **Litovski, V. B.,** and Petkovic, P. M., ”*Why does the grid needs cryptography?*” Electronics, ISSN: 1450-5843, Vol. 13, No. 1, June 2009, pp. 30-36.

c.59. Sokolović M., and **Litovski, V., “***Statistical timing analysis of asynchronous circuits using logic simulator***”,** Electronics, ISSN: 1450-5843, Vol. 13, No. 1, June 2009, pp. 37-42.

c.60. Sokolović,M., **Litovski, V.**, and Zwolinski, M., “*Efficient and realistic statistical worst case delay computation using VHDL*”, Electrical Engineering, ISSN: 0948-7921, DOI 10.1007/s00202-009-0133-y**,** Volume 91, Numbers 4-5 / December, 2009, pp. 197-210

c.61. Milojković, J, and **Litovski, V.B.,** „*Dynamic Short-Term Forecasting of Electricity Load Using Feed-Forward ANNs*“, Int. J. of Engineering Intelligent Systems for Electrical Engineering and Communication, ISSN 1472-8915, Vol. 17, No. 1, March 2009, pp. 38-48.

c.62. Andjelković, B., **Litovski, V.,** and Zerbe, V., "*Grid-enabled Parallel Simulation Based on Parallel Equation Formulation*", ETRI J. (ISSN 1225-6463), Vol. 32, No. 4, August 2010, pp. 555-565.

c.63. Milojković, J.B., **Litovski, V.B.,** “Short-term Forecasting of Electricity Load Using Recurrent ANNs”, “Electronics”, ISSN: 1450-5843, Vol. 14, No. 1, June 2010, pp. 45-49.

c.64. Đorđević, S., Petković, P., and **Litovski, V.,** „*A new topology oriented method for symbolic analysis of electronic circuits*”, J. of Circuits, Systems, and Computers, Vol. 19, No. 8, 2010, pp. 1-15.

c.65. Andrejević Stošović, M., and **Litovski, V.,** „*Hierarchical approach to*

diagnosis of electronic circuits using ANNs“, J. of Automatic Control, University of Belgrade, Vol. 20, No. 1, 2010, pp. 45-52.

c.66. Andrejević Stošović, M., and **Litovski, V.,** „*Hierarchical approach to diagnosis of mixed-mode circuits using Artificial Neural Networks*“, Neural Network World, ISSN 1210-0552, Vol. 21, No. 2, 2011, pp. 153-168.

c.67. Milojković, J.B., **Litovski, V.B.,** “*Short-term forecasting in Electronics*”, Int. J. of Electronics, ISSN: 0020-7217, Vol. 98, No. 2, 2011, pp. 161-172.

c.68. Andrejević Stošović, M., Dimitrijević, M., and **Litovski, V.,** „*New Hierarchical Grid Based Diagnosis of Electronic Circuits using ANNs*”, Int. J. of Research and Reviews in Computer Science (IJRRCS), ISSN: 2079-2557, Special Issue, Vol. 2, April 2011, pp. 10-17.

c.69. Dimitrijević, M., and **Litovski, V.,** „*Power Factor and Distortion Measuring for Small Loads Using USB Acquisition Module*”, J. of Circuits, Systems, and Computers, Vol. 20, No. 5, August 2011, pp. 867-880.

c.70. Andrejević Stošović, M., Milić, M., and **Litovski, V.,** „*Analog filter diagnosis using the oscillation based method“, J. of Electrical Engineering*, ISSN 1335-3632, last impact factor: 0.37, Vol. 63, No. 6, 2012, pp. 349–356.

c.71. Andrejević Stošović, M., , Dimitrijević, M., **Litovski, V.,** "*Computer Security vulnerability as Concerns the Electricity Distribution Grid*", Applied Artificial Intelligence, ISSN: 0883-9514 print/1087-6545 online DOI: 10.1080/08839514.2014.891831, Vol. 28, pp. 323–336, 2014, 2012 Impact Factor: 0.475, Ranking: 96/115 in Computer Science, Artificial Intelligence; 197/243 in Engineering, Electrical & Electronic, 2012 5-Year Impact Factor: 0.505

c.72. Andrejević Stošović, M., Milić, M., Zwolinski, M., **Litovski, V.**,”*Oscillation-based analog diagnosis using artificial neural networks based inference mechanism*”, COMPELECENG-D-11-00818R3, Computers and Electrical Engineering, Vol. 39, 2013, pp. 190-201. ISSN: 0045-7906, Impact Factor: 0.928.

c.73. Dimitrijević, M., Milojković, J., Slobodan Bojanić, S., Nieto-Taladriz, O., and **Litovski, V.**, “*ICT and power: new challenges and solutions*”, Int. J. Reasoning-based Intelligent Systems, Vol. 5, No. 1, 2013, pp. 32-41. Publisher: Inderscience Enterprises, ISSN: 1755-0556, E-ISSN: 1755-0564.

c.74 Topisirović, D., **Litovski, V.,** and Andrejević Stošović, M., „*Unified theory and state-variable implementation of critical-monotonic all-pole filters*“, Int. J. of Circuit Theory and Applications, Article first published online: 22 OCT 2013, DOI: 10.1002/cta.1956, ISSN: 0098-9886; IF(2012): 1.293; M22 (102/243). Vol. 43, No. 4, April 2015, pp. 502–515.

c.75 Andrejević Stošović, M., **Litovski, V.,** “*Implementation of recurrent*

artificial neural networks for nonlinear dynamic modeling in biomedical applications", Int. J. Artificial Organs, 2013, Vol. 36, No. 11, pp. 833 – 842. DOI:10.5301/ijao.5000255. impact factor: 1.964.

c.76. Dimitrijević, M., Andrejević Stošović, M., Milojković, J., **Litovski, V.,** "*Implementation of Artificial Neural Networks Based AI Concepts to the Smart Grid*", Facta Universitatis, Series: Electronics and Energetics Vol. 27, No 3, September 2014, pp. 411 - 424. DOI: 10.2298/FUEE 1403411D.

c.77. Andrejević Stošović, M., Litovski, I., Lukač, D., Dimitrijević, M., and **Litovski, V**., "*Small Signal Model of a Solar Cell",* Simulation, Trans. of the Society for Modeling and Simulation, International. Published online 1 October 2014, Oct. 01, 2014, Impact factor=0.692.
http://sim.sagepub.com/content/early/2014/10/01/0037549714551290

c.78. Andrejevic Stosovic, M.V., Živanić, J.M., **Litovski, V.B.,** *" Maximally flat filter functions with maximum number of transmission zeros having maximal multiplicity,*" IEEE Trans. on Circuits and Systems II: Express Briefs, vol.61, no.10, pp.778-782, Oct. 2014.
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6870441 &isnumber=6914631

To:
Vanco B. Litovski
Tuesday, August 04, 2015 11:03 PM

World Scientific
www.worldscientific.com

ICP Imperial College Press
www.icpress.co.uk

Dear Prof. Litovski,

Thank you for publishing with us. Your article, Standard Cell-Based Low Power Embedded Controller Design, is an important contribution to the Journal of Circuits, Systems and Computers and its subject area.

We hope to have the privilege of reviewing and publishing your next article.

Sincerely,
Journal Department
World Scientific Publishing

c.79. Mirković, D., Petković, P., and **Litovski, V.B.,** " *A second order s-to-z transform and its implementation to IIR filter design*", COMPEL: The Int. J. for Computation and Mathematics in Electrical and Electronic Eng., Vol. 33, No. 5, 2014 pp. 1831-1843.

c.80. Dimitrijević, M., Andrejević Stošović, M., and **Litovski, V.,** "*Computer Security Vulnerability Seen From the Electricity Distribution Grid Side*", Facta Universitatis, Series: Electronics and Energetics, Vol. 27, No 3, September 2014, pp. 411 – 424.

c.81. Jovanović, B., **Litovski, V.,** and Pavlović, M., "*QRS Complex Detection Based ECG Signal Artefact Discrimination*", Facta Universitatis, Series: Electronics and Energetics, Vol. 28, No 4, December 2015, pp. 571-584.

c.82. Milić, M., and **Litovski, V.,** "*Oscillation-based testing method for detecting Switch faults in high-q sc biquad filters*", Facta Universitatis, Series: Electronics and Energetics, Vol. 28, No 2, June 2015, pp. 223 - 236 DOI: 10.2298/FUEE1502223M

c.83. Jovanović, B., Damnjanović, M., Petković, P., and **Litovski, V.,** "*Standard Cell-Based Low Power Embedded Controller Design*, Journal of Circuits, Systems, and Computers, Vol. 24, No. 6, 2015, 1550077 (19 pages) DOI: 10.1142/s0218126615500772.

c.84. Mirković, D., Andrejević Stošović,M., Petković, P., and **Litovski, V.,** "*IIR digital filters with critical monotonic pass-band amplitude characteristic*", Int. J. Electron. Commun. (AEÜ), Vol. 69, 2015, pp. 1495–1505.

c.85. Mirković, D., Andrejević Stošović,M., Petković, P., and **Litovski, V.,** "*Design of IIR Digital Filters With Critical Monotonic Passband Amplitude Characteristic - A Case Study*", Facta Universitatis, Series Electronics and Energetics, Vol. 29, No 2, June 2016, pp. 269 – 283.

c.86. Andrejević Stošović, M., Dimitrijević, M., Bojanić, S., Nieto-Taladriz, O., **Litovski, V.,** "Characterization of Nonlinear Loads in Power Distribution Grid", Facta Universitatis, Series Electronics and Energetics, Vol 29, No 2, 2016, pp. 159-175.

c.87. **Litovski, V. B.,** Le Blond S. P., and Ross, B. P., "Transient circuit implementation of arc models with particular focus on arcs in low-voltage power cables", Electric Power Systems Research, Vol. 147, June 2017, pp. 105–114.

c.88. Milojković, J., **Litovski, V.,** and Le Blond, S., "Low-Voltage Circuit Breakers Based on WBG Solid-State Devices", J. of Circuits, Systems, and Computers ,Vol. 27, No. 2, 2018, pp. 1850020-1-1850020-19.

c.89. Andrejević Stošović, M., and **Litovski, V**.," Applications of Artificial Neural Networks in Electronics", Electronics, Vol. 21, No. 2, Dec. 2017, pp. 87-94.

90. Andrejević Stošović, M., Topisirović, D., & **Litovski, V.,** "Frequency and time domain comparison of selective polynomial filters with corrected phase characteristics", Int. J. of Electronics, Published online: 13 Feb 2019. DOI: 10.1080/00207217.2019.1570560, Vol. 106, 2019, No. 5, pp. 770-

784.

d. Paper published i domestic journals in Serbian (marked by asterix) **and English**

d.1.* **Litovski, V.**, *"Filtri sa maksimalno zaravnjenom karakteristikom grupnog kašnjenja i jedna nova klasa filtara sa dobrim grupnim kašnjenjem"*, Naučni podmladak, Vol. 2, 1970, pp. 115-126.

d.2.* **Litovski, V.**, *"Granično monotona amplitudna karakteristika sa konačnim nulama prenosa i maksimalnim nagibom na granici propusnog opsega"*, Tehnika (Elektrotehnika), Vol. 26, No. 2, 1977, YU ISSN 0040-2176, pp. E1-E3.

d.3.* **Litovski, V.**, Petrović, G., *"Sinteza filtarske ćelije drugog reda sa proizvoljnim rasporedom nula prenosa"*, Tehnika (Elektrotehnika), Vol. 27, No. 7-8, 1978, YU ISSN 0040-2176, pp. E1-E3.

d.4.* Lazović, S., **Litovski, V.**, *"Karakteristike niskofrekventnih monotonih filtara za linijske skretnice"*, Zbornik radova Saobraćajnog fakulteta, Vol. 28, No. 4, 1979, pp. 49-93.

d.5.* **Litovski, V.**, Mitić, P., *"Sinteza prenosnih funkcija selektivnih filtara propusnika opsega s linearnom faznom karakteristikom"*, Tehnika (Elektrotehnika), Vol. 29, No. 1, 1980, YU ISSN 0040-2176, pp. E1-E6.

d.6.* **Litovski, V.**, Jevtić, M., Pantić, S., *"Uticaj nesavršenosti operacionih pojačavača na karakteristike niskopropusnih filtara"*, Tehnika (Elektrotehnika), Vol. 29, No. 10, 1980, YU ISSN 0040-2176, pp. E7-E12.

d.7.* **Litovski, V.**, Stanković, T., *"Simulacija prelaznih režima u električnim kolima sa magnetima sa pokretnom kotvom"*, Elektronika (Nauka i praksa), Vol. 1, Br. 1, 1981, pp. 16-21.

d.8.* Milovanović, D., **Litovski, V.**, *"Fazni korektori u električnim filtrima neminimalne faze"*, Tehnika (Elektrotehnika), Vol. 31, No. 6, 1982, YU ISSN 0040-2176, pp. 1025-1028.

d.9.* Stanojević, S., **Litovski, V.**, *"Simbolička analiza električnih kola"*, Tehnika (Elektrotehnika), Vol. 31, No. 12, 1982, YU ISSN 0040-2176, pp. 1895-1989.

d.10.* Damnjanović, M., **Litovski, V.**, *"Realizacija jednog algoritma za projektovanje veza u integrisanim kolima"*, Automatika, Zagreb, Vol. 23, No. 1-2, 1982, pp. 47-53.

d.11.* Milenković, S., **Litovski, V.**, *"Kolo za trostepenu regulaciju boje tona"*, Naučni podmladak, Vol. XVIII, No. 1-2, Univerzitet u Nišu, 1986.

d.12. **Litovski,V.**, *"LIFT - računarski program za analizu linearnih elektronskih kola "*, Elektrotehniški vestnik, Ljubljana, Vol. 53, No. 4-5,

1987, pp. 287-293.
d.13.* **Litovski, V.**, Milenković, S., Milićević, M., *"Generisanje inicijalnog razmeštaja u gejtovskoj matrici GEM21"*, Tehnika (Elektrotehnika), Vol. 36, No. 10, 1987, YU ISSN 0040-2176, pp. 957-960.
d.14.* **Litovski, V.**, Petković, P., Milenković, S., *"Analiza MOS integrisanih kola upotrebom programa MOST II"*, Elektronika (nauka i praksa), Vol. 8, No. 1/2, Jun, 1988, pp. 3-14.
d.15.* Damnjanović, M., **Litovski, V.**, *"Jedno rešenje povezivanja u gejtovskoj matrici GEM 21"*, Elektrotehnika (Tehnika), Vol. 37, No. 3, 1988, YU ISSN 0040-2176, pp. 337-340 (e1-e4).
d.16.* Ilić, S., **Litovski, V.**, *"Simulacija tiristorskog invertora u kolu za generisanje visokog napona u rentgenskim uredjajima"*, Elektrotehnika (Tehnika), Vol. 37, No. 2, 1988, YU ISSN 0040-2176, pp. 221-227 (e13-e19).
d.17. Janićijević, I., Radenković, Z., Janković, T., **Litovski, V.**, *"Experiences With Gks-Equivalent Software Development For 16-Bit Machines"*, (štampano u zborniku -"Automatika-appendix" posle recenzije radova sa Konf.: "The Third Int. Conf. on Computer Graphics"), 22-24 june, 1988, Automatika, Zagreb, Vol. 29, No. 1-2, pp. a.357-a.362.
d.18.* Mrčarica, Ž., **Litovski, V.**, Petković, P., *"Izbor modela kratkokanalnog MOS tranzistora za simulaciju elektronskih kola"*, Tehnika (Elektrotehnika), Vol. 40, No. 5-6, 1991, YU ISSN 0040-2176, pp. e1-e5.
d.19.* Glozić, D., **Litovski, V.**, *"ASCOTA2 - program za automatsko projektovanje CMOS operacionih pojačavača"*, Tehnika (Elektrotehnika), Vol. 40, No. 7-8, 1991, YU ISSN 0040-2176, pp. e1-e7.
d.20.* Radenković, Z., **Litovski, V.**, *"Z-R kompakcija podržana znanjem"*, Tehnika (Elektrotehnika), Vol. 42, No. 4, 1993, YU ISSN 0040-2176, pp. e6-e11.
d.21. Zarković, K., Ranđelović, Z., Milenković, S., Novaković, M., Jovanović, Lj., **Litovski, V.**, *"JUDGE - Jacquard Developing Environment (Editor)"*, Tekstilna industrija, No. 3-4/97, Beograd, 1997.
d.22.* Janković, S., Maksimović, D., Živković, V., Petković, P., **Litovski, V.**, "*Testabilno digitalno integrisano kolo specifične namene sa ugradjenim analognim multiplekserom*", Elektronika, Vol. 1, No. 1, Decembar, 1997, pp. 56-60.
d.23.* Maksimović, D., Janković, S., **Litovski, V.**, "*Alecsis: Modeliranje i predikcija perfomansi digitalnih VLSI kola*", Tehnika (Elektrotehnika), Vol. 47, No. 2, 1998, YU ISSN 0040-2176, pp. E6-E20.
d.24.* Maksimović, D., **Litovski, V.**, "*Analiza topoloških kašnjenja u digitalnim kolima pomoću logičkog simulatora*", Tehnika (Elektrotehnika), Vol. 48, No. 2, 1999, YU ISSN 0040-2176, pp. E1-E13.

d.25.* Maksimović, D., Panić, V., Zarković, K., Petković, Z., Milovanović, D., Topisirović, D., **Litovski, V.,** "*Implementacija digitalnih elektronskih kola primenom boundary scan standarda*", Tehnika (Elektrotehnika), Vol. 50, 2001, YU ISSN 0040-2176, pp. E7-E15.

d.26.* Andrejević, M., **Litovski, V.,** "*Primena veštačkih neuronskih mreža za modelovanje reaktivnih nelinearnih dvopola*", Tehnika (Elektrotehnika), Vol. 51, No. 4-5, Maj 2002, YU ISSN 0040-2176, pp. E1-E11.

d.27.* Maksimović, D., and Litovski, V.B., „*Upotreba VHDL simulatora za timing simulaciju*“, TEHNIKA, Elektrotehnika, YU ISSN 0040-2176, Vol. 51, No. 3/4, 2002, pp. 1-8.

d.28.* Stefanović, D., Kayal M., **Litovski V.**, “*Proceduralno projektovanje analognih CMOS integrisanih kola na primeru Milerovog operacionog pojačavača*”, Tehnika (Elektrotehnika), Vol. 52, No. 2, 2003, YU ISSN 0040-2176, pp. 8-17.

d.29. Jovanović. B., Damnjanović, M., i **Litovski, V.**, «*Square Root on Chip*”, ETF J. of Electrical Engineering, A Publication of the EE Department, University of Montenegro May 2004 Vol.12 No.1 YU ISSN: 0353-5207

d.30.* Dimitrijević, M., i **Litovski V.**, “*Laboratorija za elektroniku podržana računarskom mrežom*”, Tehnika (Elektrotehnika), Vol. 55, No. 3, 2006, YU ISSN 0040-2176, pp. E.3-E.9.

d.31.* Milojković, J., i **Litovski V.**, “*Postupci predviđanja količina elektronskog otpada od računara*”, Tehnika (Elektrotehnika), Vol. 56, No. 1, 2007, pp. E.7-E.16.

d.32. Milić, M, and Litovski, V.,"*Statistical Delay Estimation in Digital Circuits Using VHDL*",Technics, Electrical Engineering,Vol. 63 , 2014, Special edition, ISSN 0013-5836, pp. 71-78.

5.e. Invited papers published at international conferences

e.1. **Litovski, V.**, *"An Integrated System For Gate-Array Design"*, Proc. of the Int. Symposium: Hybrid and Semiconductor Technology, Gate-Arrays and Semiconductor Lasers, Sozopol, May, 1988, pp. 25-67. Invited paper

e.2. Damnjanović, M., **Litovski, V.**, "*Routing Algorithms In Custom Ic Design*", Proc. of the 2nd Hungarian Custom Circuits Conf., CCC 89., Szeged, 10-12 Maj, 1989, pp. 83-111. Invited paper

e.3. **Litovski, V.**, *"New Results In Integrated Software Development For Gate-Array Design"*, Proc. of the 3rd MidEuropean Custom Circuit Conf., Sopron, 21-24 April, 1991, pp. 69-83. Invited paper

e.4. **Litovski,V.**, *"New Tehnologies in the Design of Integrated Electronic Circuits"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics,

MIOPEL '93, Niš, 26-28 Oktobar, 1993, pp. 383-399. Invited paper

e.5. Zwolinski, M., **Litovski, V.**, *"Hybrid Simulation: The State-Of-The-Art"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, Srbija, 26-28 Oktobar, 1993, pp. 375-382. Invited paper

e.6. Milenković, S., **Litovski, V.**, Obradović, Z., *"A New Adaptive Move Type Selection In Simulated Annealing"*, 15-16 Int. Anual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 22-31. Invited paper

e.7. Pantić, D., Milenković, S., Trajković, T., **Litovski, V.**, Stojadinović, N., *"Inverse Modeling Of Semiconductor Manufacturing Processes"*, 20th Int. Conf. on Microelectronics MIEL '95, Vol. 1, Niš, 12-14 Sep., 1995, pp. 321-326. Invited paper

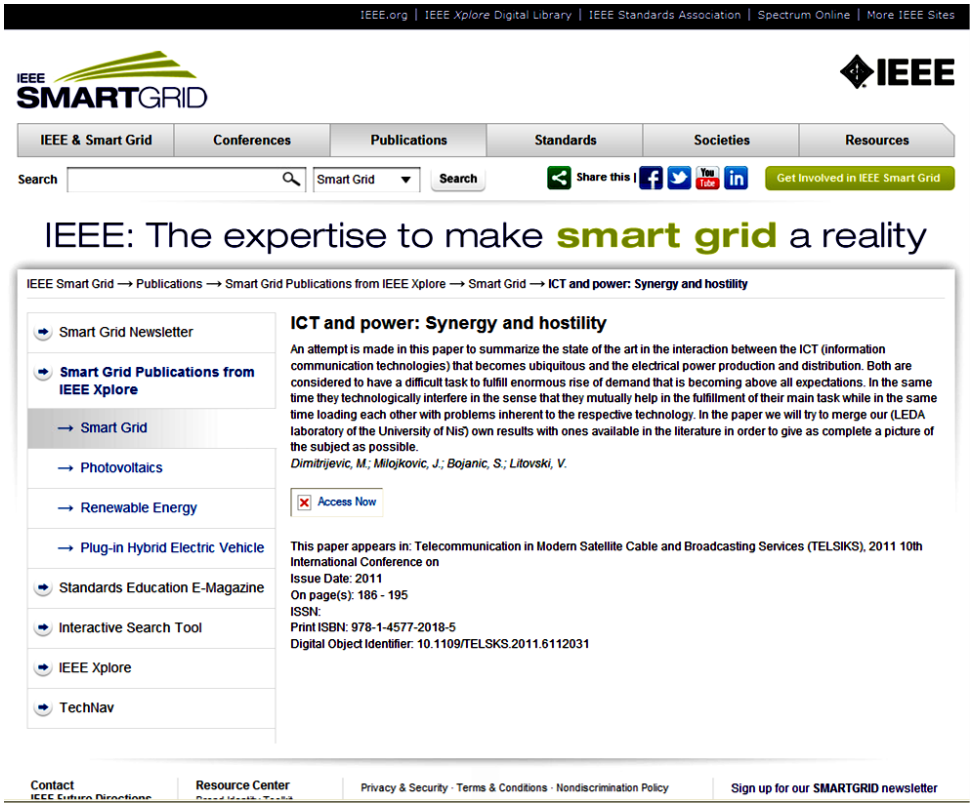
e.8. **Litovski, V.**, Ranđelović, Z., Damnjanović, M., *"Routing In Standard Cells"*, 20th Int. Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 461-466. Invited paper

e.9. Petković, P., Milovanović, D., **Litovski, V.**, *"Symbolic Function Extraction And Fault Modelling Of MOS Circuits"*, 20th Int. Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 473-478 Invited paper.

e.10. Andrejević, M., **Litovski, V.,** "*Electronic Modelling Using ANNs For Analogue and Mixed-Mode Behavioural Simulation*", Proc. of NEUREL 2002, 2002, Belgrade, pp. 113-118. Invited paper

e.11. Sokolović, M., Zwolinski, M., and **Litovski, V**., "*New Concepts of Worst-case Delay Evaluation in Asynchronous VLSI SoC*", PROC. 26th Int. Conf. on Microelectronics (MIEL 2008), Niš, Serbia , 11-14 May, 2008, pp. 377-385. Invited paper

e.12. Dimitrijević, M., Milojković, J., Bojanić, S., and **Litovski, V.,** "*ICT and Power: Synergy and Hostility*", Proc. of the 10th Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services, TELSIKS 2011, Niš, Serbia, ISBN: 978-1-4577-2017-8, pp. 186-194, Invited paper.



e.13. Andrejević Stošović, M., Lukač, D., and **Litovski, V.**, „*Modeling and circuit simulation of photovoltaic cells – an overview*“, 7th Int. Symp. „Nikola Tesla“, Belgrade, Serbia, Nov. 2011, pp. 83-92. ISBN 987-86-7466-420-9.

e.14 Le Blond, S., and Litovski, V. B., “A mechanism for collaboration between industry and academia in the UK, exemplified by project SYNAPS”, Proc. of the 6th Small Systems Simulation Symposium, SSSS'14, Niš, 2016, ISBN 978-86-6125-154-2, pp. 1-7

5.f. Invited papers published at domestic conferences (Papers written in Serbian are marked by an asterix)

f.1.* Zarković, K., Milenković, S., Glozić, D., **Litovski, V.**, *"Novi rezultati u primeni neuronskih mreža za modeliranje i simulaciju elektronskih kola"*, 3rd Seminar on Neural Network Applications in Electrotechnics, NEUREL-95, 29-30 Sep., 1995, pp. 108-116.

f.2.* **Litovski, V.**, Aleksić, D., Milenković, S., "*Simulacija računarskih mreža*", Šesnaesti Simp. o novim tehnologijama u poštanskom i

telekomunikacionom saobraćaju, Beograd, 1998.

f.3.* **Litovski, V. B**., «*Razvoj sekcije "Elektronika" u okviru konferencije ETRANa - prvih 50 godina*», L Konferencija ETRANa, Beograd, Juni 2006. god., pp. EL, 1, 5-8.

f.4.* Jelena Milojković, Vančo Litovski, "*Predviđanje Maksimuma Dnevne Potrošnje Električne Energije Pomoću Veštačkih Neuronskih Mreža*", Naučno-stručni simpozijum Energetska efikasnost, ENEF 2013, Banja Luka, Nov. 2013, pp. B1-16-B1-21.

5.g. **Papers published at international conferences**

g.1. Lazović, S., **Litovski, V.**, *"A New Method Of Band-Pass Allpass Network Synthesis For Compression"*, Proc. of the II Int. Symposium on Network Theory, Herceg-Novi, 1971, pp. 275-284.

g.2. **Litovski, V.**, *"Lowpass Filter Design Using Complex Transmission Zeros"*, Proceedings of the 23. Intern. Wiss. Koll. TH, Ilmenau, 1978, pp. 29-32.

g.3. **Litovski, V.**, *"Computer And Electronic Simulation Of Ring Waterwork Systems"*, Proceedings of the 24. Intern. Wiss. Koll. TH, Ilmenau, 1979, pp. 133-136.

g.4. **Litovski, V.**, *"Transient Simulation In Circuits With MOS Transistors"*, Proc. of the 27. Intern. Wiss. Koll. TH, Ilmenau, 1982, pp. 237-240.

g.5. **Litovski, V.**, Petković, P., *"Time Domain Temperature Dependence Simulation Of MOS Electronic Circuits"*, Proc. of the 6th Int. Conf. on computers in design engineering, CAD84, Brighton, April, 1984, pp. 61-66.

g.6. **Litovski, V.**, Pantić, S., *"LANA: Fortran Subroutine For MOS-Transistor-Model Implementation In Circuit-Analysis Program"*, Proc. of the 7th European conf. on Electrotechnics, EUROCON 86, Paris, april, 1986, pp. 436-441.

g.7. Petković, P., **Litovski, V.**, *"Macromodeling and Macroanalysis of CMOS LSI Electronic Circuits"*, Proc. of the Conf. on VLSI and Computers, COMPEURO 87, Hamburg, May, 1987, pp. 512-513.

g.8. **Litovski, V.**, Milovanović, D., Stojanović, Z., *"LOSTIN - A Computer Program For Communication With A Gate Level Logic Simulator"*, Proc. of the 32 Int. Wiss. Kolloq. der TH Ilmenau, October, 1987 , pp. 215-218.

g.9. **Litovski, V.**, Petković, P., *"Time Domain Black-Box Modelling Of CMOS Structures And Analog Timing Simulation"*, 3rd Annual European Computer Conf., COMPEURO '89, Hamburg, May, 1989, pp. 5.142-5.143.

g.10. **Litovski, V.**, Gmitrović, M., *"Interconnect Modelling And Simulation In VLSI"*, Proc. of the VII Int. Conf. on Microelectronics,

MICROELECTRONICS '90, Minsk, October, 1990, pp. 21-22.
g.11. Damnjanović, M., **Litovski, V.**, *"Global And Detailed Automatic Routing In A Gate-Array"*, Proc. of the 35. Int. Wiss. Kolloquium, Ilmenau, 22-26 October, 1990, pp. 25-28.
g.12. Milovanović, D., **Litovski, V.**, *"New CMOS Transmission Gate Fault Models And Fault Simulation"*, Proc of the Int. Conf. on Concurrent Engineering and Electronic Design Automation, CEEDA '91, Poole, March, 1991, pp. 393-395.
g.13. Petković, P., **Litovski, V.**, *"Output Resistance Of CMOS Logic Cells"*, Proc. of the 3rd Mideuropian CCC 1991, Sopron, Hungary, April, 1991, pp. 237-244.
g.14. Milenković, S., **Litovski, V.**, *"Analytical Approach To The Placement Problem In Gate-Arrays"*, IEEE COMPEURO '91, Bologna, Italy, May, 1991, pp. 800-804.
g.15. Mrčarica, Ž., **Litovski, V.**, *"Some Considerations Of Short-Channel MOS Model Selection For An Analog Circuit Simulation Program"*, Microsystem '92, Bratislava, 17-19. November, 1992.
g.16. Glozić, D., **Litovski, V.**, Petković, P., *"ADIL: - Analog Design Instruction Language For More Flexible Simulation In Synthesis Process"*, EUROSIM '92, Capri, 28.9-2.10, 1992, pp. 453-458.
g.17. **Litovski, V.**, *"Simulated Intelligence And The Design Of Electronic Circuits"*, 37. Internationales Wissenschaftliches Kolloquium, Ilmenau, 21-24.9, 1992.
g.18. **Litovski, V.**, Pantić-Tanner, Z., *"Artificial Neural Network Application In Electronic Circuit Analysis"*, World Congress On Neural Networks, Portland, Oregon, 11-15 July, 1993.
g.19. Milovanović, D., **Litovski, V.**, *"Modeling Procedures For BiCMOS Cells"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 Oktober, 1993, 421-425.
g.20. Milovanović, D., **Litovski, V.**, and Obradović, M., *"A Review Of Fault Models Of BiCMOS Cells"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 October, 1993, pp. 415-420.
g.21. Damnjanović, M., **Litovski, V.**, *"CAD Systems Based On VHDL Description"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 October, 1993, pp. 443-448.
g.22. Petković, P., Stevanović, R., **Litovski, V.**, *"Symbolic Approach to Linear Circuit Analysis"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 October, 1993, pp. 437-442.
g.23. Milenković, S., **Litovski, V.**, *"A New Adaptive Generation Strategy In Simulated Annealing"*, European Conf. in Circuit Theory and Design, ECCTD '93, Davos, 30.8-3.9, 1993.

g.24. Ranđelović,Z., **Litovski,V.**, *"An Application Of Hopfield-Tank's Neural Net On Chanel Routing"*, 15-16 Int. Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 106-111.

g.25. Petković, P., **Litovski, V.**, *"Linear Circuit Analysis Based On Symbolic Algebra"*, 15-16 Int. Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 112-120.

g.26. Milovanović, D., **Litovski, V.**, *"Logic Models Of CMOS Transmission Gate With A Floatin-Gate Transistor"*, 15-16 Int. Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 126-132.

g.27. Maksimović, D., Glozić, D., **Litovski, V.**, *"Logic Simulation Modeling Techniques In Hybrid Simulator Alecsis2.0"*, 15-16 Int. Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 133-139.

g.28. Milovanović, D., **Litovski, V.**, Jevtić, M., *"Fault Modeling Of MSD Flip-Flops"*, 17th Edition of Annual Semiconductor Conf., CAS '94, Proceedings Volume 2, Sinaia, 11-16 Oct., 1994, pp. 401-404.

g.29. Maksimović, D., Glozic, D., **Litovski, V.**, *"Discrete Event Modeling And Simulation In An Object Oriented Hybrid Simulator"*, XIV IASTED Int. Conf.: Modelling Identification and Control, Innsbruck, Feb., 1995, pp. 103-106.

g.30. Ranđelović, Z., Milenković, S., **Litovski, V.**, *"Global Routing For The Standard Cell Layout"*, Annual School - 17th Int. Spring Seminaron Semicoductor and Hybrid Technologies 1994-1995, Sozopol, 1995, pp. 248-254.

g.31. Janković, S., Milovanović, D., **Litovski, V.**, *"Experiences In Using The System Magic For Designing IC"*, Annual School - Int. Spring Seminar on Semicoductor and Hybrid Technologies 1994-1995, Sozopol, 1995, pp. 242-247.

g.32. Dimić, Ž., Damnjanović, M., Glozić, D., **Litovski, V.**, *"VHDL Use For Alecsis Hybrid Simulation"*, Annual School - 17th Int. Spring seminar on Semiconductor and Hybrid Technologies 1994-1995, Sozopol, 1995, pp. 228-241.

g.33. Mrčarica, Ž., Ilić, T., Glozić, D., Detter, H., **Litovski, V.**, *"Mechatronics Simulation Using Alecsis, Anatomy Of Simulator"*, EUROSIM '95, Vienna, 1995, pp. 601-604.

g.34. Mrčarica, Ž., Glozić, D., Ilić, T., **Litovski, V.**, *"Capacitive Preassure Sensor For Quasi-Static Conditions Followed By A/D Conversion"*, 20th Int. Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12.-14. Sep., 1995, pp. 601-604.

g.35. Panić, V., Milovanović, D., Petković, P., **Litovski, V.**, *"Fault Location In Passive Analog RC Circuits By Measuring Impulse Response"*, 20th Int. Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 517-520.

g.36. Damnjanović, M., Dimić, Ž., **Litovski, V.**, Glozić, D., *"Hardware Description Language For Alecsis Simulator"*, 20th Int. Conf. on Microelectronics, MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 525-528.

g.37. Petković, P., Marković, V., **Litovski, V.**, *"Application Of A Symbolic Simulator In The Education Process"*, 8th Int. Symp. on Theoretical Electronic Engineering, ISTET '95, Thessaloniky, 22-23 Sep., 1995, pp. 529-532.

g.38. Mrčarica, Ž., Glozić, D., **Litovski, V.**, Detter, H., *"Simulation Of Microsystems Using A Behavioural Hybrid Simulator Alecsis"*, First Int. Conf. on Microsystems and Microstructures, MICROSIM'95, Southampton, 26-28 Sep., 1995, pp. 129-136. Preštampano u celosti u: Adey, R.A., Lahrmann, A., Lemboe Ilmann, C., editors, "Simulation and Design of Microsystems and Microstructures" , Computational Mechanics Publication, Southampton, GB, 1995. Takođe odštampano u celosti u: Transactions on the Built Environment, Vol 12, © 1995 WIT Press, www.witpress.com, ISSN 1743-3509.

g.39. Milenković, S., Obradović, Z., **Litovski, V.**, *"Annealing Based Dynamyc Learning In Second-Order Neural Networks"*, IEEE Int. Conf. on Neural Networks ICNN '96, ISBN: 0-7803-3210-5, Washington, D.C., 3.-6. June, 1996, pp. 458-463.

g.40. Marković, V., Petković, P., **Litovski, V.**, *"Symbolic Approach To The Microwave Circuit Design"*, XI Int. Microwave Conf. MICON '96, Warsaw, 27-30 May, 1996.

g.41. Ranđelović, Z., **Litovski, V.**, Radović, O., *"Ekspertni sistemi za povezivanje u kanalu"*, Prvi međunarodni Simp.: Industrijsko inženjerstvo '96, Beograd, 1996, pp. 522-524.

g.42. **Litovski, V.**, Zwolinski, M., Litovski, I., *"Large-Change-Sensitivity Computation In Linear Electronic Circuits"*, Proceedins of 18th Int. Spring Seminar on Semiconductor and Hybrid Technologies, Sozopol, 1996, pp. 268-274.

g.43. Milovanović, D., **Litovski, V.**, *"Modeling Procedures And Fault Models Of BiCMOS Logic Circuits"*, Proceedings of 18th Int. Spring Seminar on Semiconductor and Hybrid Technologies, Vol. 1, Sozopol, 1996, pp. 285-293.

g.44. Rađenović-Mrčarica, J., Mrčarica, Ž., Detter, H., Brenner, W., **Litovski, V.**, *"Neural Network Visual Recognition Applied To Microelectromechanical Parts Assembly"*, Int. Conf. on Engineering

Applications of Neural Networks, EANN '96, Kingston upon Thames, 1996, pp. 325-328.

g.45. Mrčarica, Ž., Detter, H., Glozić, D., **Litovski, V.**, *"Describing Space-Continous Models Of Microelectromechanical Devices For Behavioural Simulation"*, European Design Automation Conf., EURO-DAC '96 with EURO-VHDL '96, Geneva, 16-20 Sep., 1996, pp. 316-321.

g.46. Mrčarica, Ž., **Litovski, V.**, Delić, N., Detter, H., *"Modelling Of Micromechanical Devices Using Hardware Description Language"*, 5th Int. Conf. and Exhibition on Micro, Electro, Opto, Mechanical Systems and Components, Microsystem Technologies '96, Potsdam, 17-19 September, 1996, pp. 293-298.

g.47. Milenković, S., **Litovski, V.**, Obradovic, Z., *"Nondeterminism In Artificial Neural Networks"*, Int. Memorial Conf. D. S. Mitrinovic, Niš, 20-22 Jun, 1996.

g.48. Keroe, N., Janković, S., Fallman, W., **Litovski, V.**, *"A High Speed Serial Bus Controller ASIC"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 737-740.

g.49. Janković, S., Maksimović, D., Petković, P., **Litovski, V.**, *"Testable Design Of Digital ASIC With Embedded Analog Multiplexers"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 779-782.

g.50. Mrčarica, Ž., **Litovski, V.**, Jakovljević, M., Detter, H., *"Hierarchical Modelling Of Microsystems In An Object-Oriented HDL"*, 21st Int. Con. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 475-478.

g.51. Dimić, Ž., Damnjanović, M., **Litovski, V.**, *"VHDL - Alec++ Co-simulation"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 725-728.

g.52. Mrčarica, Ž., **Litovski, V.**, Živković, V., *"Delay Time And Crosstalk Simulation in CMOS Integrated Circuits"*, 3rd Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services TELSIKS '97, Niš, Oct., 1997, pp. 122-125.

g.53. Rađenović-Mrčarica, J., Mrčarica, Ž., **Litovski, V.**, Detter, H., *"Application Of Neural Networks In Microsystem Assembly"*, 4th Seminar on Neural Network Applications in Electrical Engineering, NEUREL '97, Belgrade, Sep., 1997, pp. 157-160.

g.54. Milenković, S., Risojević, V., **Litovski, V.**, *"Noise Based Gradient Descent Learning"*, Proc. of 4th Seminar on Neural Networks Appl. in Electrical Engineering, NEUREL '97, Belgrade, Sep., 1997, pp. 28-33.

g.55. Mrčarica, Ž., Ranđelović, Z., Jakovljević, M., **Litovski, V.**, Detter, H., *"Methods For Description Of Microelectromechanical Device Models For System-Level Simulation"*, in Adey,R.A. and Renaud,Ph., ed. "Microsim II, Sec. Inter. Conf. on the Simulation and Design of Microsystems and

Microstructures, Proceed.", Lausanne, Sep., 1997, pp. 271-280.

g.56. Mrčarica, Ž., **Litovski, V.**, Ilić, T., *"Simulation Of The Pressure Sensor Interaction With Its Electronic Environment"*, Micromechanics Europe 1977, Eighth Workshop on Micromachining, Micromechanics and Microsystems, MME '97, Southampton, Kingdom, 31 Aug. - 2 Sep., 1997, pp. 246-249.

g.57. Aleksić, D., **Litovski, V.**, Milenković, S., *"TCP/IP Protocol Modeling And Simulation Using Alecsis 2.3"*, 3rd Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services TELSIKS '97, Niš, Oct. 1997, pp. 564-567.

g.58. Dokić, B., **Litovski, V.**, Panić, V., *"Novel BiCMOS Driver With Positive Feedback"*, 3rd Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services TELSIKS '97, Niš, Yugoslavia, 8-10 Oct., 1997, 126-129.

g.59. Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., **Litovski, V.**, "*Implementation Of Finite Elements Using An A-HDL Environment*", Numerische Simulation in Feinwerk-/Mikrotechnik und Elektronik, Muenchen, Germany, 4-5 Mart, 1998.

g.60. Damnjanović, M., **Litovski, V.**, Nikolić, D., Vučković, M., "*CMOS Standard Cell Library Design For Alliance Environment*", Electrical Engineering and Electronics '98, Gabrovo, Dec., 1998, pp. 136-141.

g.61.* Milovanović, D., **Litovski, V.**, "*Komparativni prikaz metoda testiranja CMOS integrisanih kola*", Drugi Simp. Industrijska Elektronika, INDEL '98, Banja Luka, Sep., 1998, pp. 56-59.

g.62. Milovanović, D., **Litovski, V.**, "*Iddq Versus Vddt Testing - A Comparative Study*", Electrical Engineering and Electronics, EE '98, Gabrovo, Dec., 1998, pp. 131-135.

g.63. Petković, P., **Litovski, V.**, Milovanović, D., Panić, V., "*Symbolic Oriented Function Extraction And Fault Modelling Of Analog And Digital Circuits*", Electrical Enineering and Electronics, EE '98, Gabrovo, Dec., 1998, pp. 119-124.

g.64. Đorđević, S., Živković, V., **Litovski, V.**, Petković, P., "*Determination Of Boundaries Between Frequency Segments During Segmented Symbolic Simulation*", Electrical Engineering and Electronic, EE '98, Gabrovo, Dec., 1998, pp. 125-130.

g.65. Keroe, N., Janković, S., Fallmann, W., **Litovski, V.**, "*Automatisierter Entwurfs Eines Seriellen Hochgeschwind- igkeits-Bus-Controller-Asics*", Proceedings of AUSTROCHIP '98, Viena, Austria, 1998, pp. 78-82.

g.66. Shutinoski, G., Dzhekov, T., **Litovski, V.**, "*Motion Perception Via Two Channels Correlation Mechanism: VLSI Proposal For An Object Tracking System Implementation*", Preprints of the IFAC Workshop on Intelligent

Components for Vehicles, ICV '98, Seville, March, 1998, pp. 41-46. Published by Pergamon.

g.67. Shutinoski, V.G., Dzhekov, T.A. and **Litovski, V.B.,** "*Current Mode VLSI Neuromorphic Cell Proposal for Motion Detection*", 42nd MWSCAS, Las Cruces, New Mexico, Aug. 1999, coll. abstracts p. 189.

g.68. Shutinoski, V.G., Dimirovski, G.A., and **Litovski, V.B.** "*Current Mode VLSI Neural Network for Motion Perception*", Proc. of the 3rd IEEE Int. Conf. on Intelligent Engineering Systems, INES'99, Star Lesn, Slovakia, November, 1999.

g.69. Mrčarica, Ž., Risojević, V., Lenczner, M., Jakovljević, M., **Litovski, V.**, "*Integrated Simulator For Mems Using FEM Implementation In AHDL And Frontal Solver For Large Sparse Systems Of Equations*", Design, Test and Microfabrication of MEMS, MOEMS '98, CAD, Design and Test, Paris, 30. Mar. - 1. Apr., 1999, pp. 306-315.

g.70. Maksimović, D., **Litovski, V.**, "*Inverse Circuit Simulation Method For Topological Delays Estimation With Logic Simulator*", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, May, 2000, pp. 707-710.

g.71. Petković, P., Đorđević, S., **Litovski, V.**, "*A New Approach To Symbolic Analysis Of Large Circuits*", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 687-690.

g.72. Panić, V., Janković, S., Milovanović, D., **Litovski, V.**, "*Cell Design for Boundary-Scan Implementation* ", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 719-722.

g.73. Ilić, T., **Litovski, V.**, "*Computationally Efficient Parametric Yield Estimation of Linear Electronic Circuits* ", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 683-686.

g.74. Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., **Litovski, V.**, "*Analogue Behavioural Simulator as a Tool for Coupled Electro-Thermal Analysis of Microsystems*", Proc. of the 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 561-564.

g.75. Zarković, K., Ilić, T., Savić, M., and **Litovski, V.**, "*ANN application in Modeling of Dynamic Two-Terminal Linear Circuits*", Proceeding of ETAI'2000, September 2000, Ohrid, pp. E-27-E-30.

g.76. Mrčarica, Ž., Maksimović, D., Tasić, A., and **Litovski, V.**, "*Some features of analogue and Mixed-Signal HDL AleC++*", Proceedings of SSSS2000, Niš, September 2000, pp. 37-42.

g.77. Jakovljević, M., Fotiu, P., Mrčarica, Ž., **Litovski, V.,** and Detter, H., "*Electro-thermal simulation of microsystems with mixed abstraction modelling*", Proceedings of SSSS2000, Niš. Sept. 2000, pp. 13-22.

g.78. Ilić, T., Zarković, K., **Litovski, V**., and Damper, R., "*ANN Application in Modelling of Dynamic Linear Circuits*", Proceedings of SSSS2000, Niš.

Sept. 2000, pp. 43-47.
g.79. Petković, P., Bushehri, E., Milenković, S., and **Litovski, V.**, "*A high level simulation for* $\Sigma\Delta$ *Modulator Design*", Proceedings of SSSS2000, Niš. Sept., 2000, pp. 53-56.
g.80. Shutinoski, G.V. Dzhekov, T.A. **Litovski, V.B.** , "*Current mode elementary motion perception neural cell*", Proc. of the IEEE Int. Symp. on Circuits and Systems, ISCAS 2000, Volume: 3, pp. 157-160, Vol.3, May 2000, Geneva, Switzerland, ISBN: 0-7803-5482-6.
g.81. **Litovski, V.,** Savić, M., "*Circuit-theoretical approach to feedback system analysis*", Electronics ET2001, Sofia, Sept., 2001, pp. 47-52.
g.82. Stefanović, D., Sokolović, M., Petković, P., and **Litovski, V**., "*TSpice-Alecsis Co-simulation*", Proceedings of MIEL'02, Niš, 2002, pp. 625-628.
g.83. Andrejević, M., Milovanović, D., Petković, P., **Litovski,** V., "*Extraction of Frequency Characteristics of Switched-Capacitor Circuits Using Time-Domain Analysis*", Proceedings of MIEL'02, Niš, 2002 pp. 635-638.
g.84. Maksimović, D., **Litovski, V.,** "*Timing Simulation With VHDL Simulators*", Proceedings of MIEL'02, Niš, 2002, pp. 655-658.
g.85. Andrejević, M., **Litovski, V.**, "*ANN Application In Modelling of Chua's Circuit*", Proc. of Neurel 2002, Belgrade, Sept. 2002, pp. 119-122.
g.86. Andrejević, M., **Litovski, V.,** "*Non-Linear Dynamic Network Modelling Using Neural Networks*", Int. Congress on Computional and Applied Mathematics, Leuven, Belgium, 22.July-26.July, 2002, pp. 16.
g.87. **Litovski, V.,** Damnjanović, M., Andjelković,B., "*ALECSIS/VHDL–AMS Mixed Language Simulation*", Proc. of the 11th Int. Scientific and Appl. Sci. Conf. Electronic ET2002, Sozopol, Sep., 2002. Vol. 1, pp. 25-30
g.88. Stefanović D., Pastre, M., Kayal, M., and **Litovski, V.,** "*Chart Oriented CAD Tool for CMOS Transistor Sizing*", Proc. of the 11th Int. Scientific and Appl. Sci. Conf. of Electronics ET2002, Sep., 2002, Sozopol, Vol. 2, pp. 95-100
g.89. Savić, M., **Litovski, V**., "*Frequency Domain Electronic Circuit Analysis in an Object Oriented Environment*", Proc. of the 11th Int. Scientific and Appl. Sci. Conf. of Electronics ET2002, Sep., 2002, Sozopol, 2002. Vol. 2, pp. 65-70
g.90. Stefanović, D., Kayal, M., Paste, M., **Litovski, V. B.,** "*Procedural Analog Design (PAD) Tool*", IEEE ISQED 2003, 4th Int. Symp. on Quality Electronic Design, 24-26 March 2003, San Jose, California, pp. 313-318
g.91. Milojković, J., Jovanović, S., **Litovski, V.,** "*Information Infrastructure for Sustainable Product Design System*", Proc. Colloquium e-Ecological Manufacturing, 2003, Berlin, pp. 75-77
g.92. **Litovski V.**, Andrejević M., Damper. R., "*Modeling the d/a interface*

for mixed-mode behavioral simulation", EUROCON 2003, Ljubljana, Sept. 2003, pp. A130-A133.

g.93. Andrejević, M., and **Litovski, V.,** *"ANN application in electronic diagnosis - Preliminary results"*, Proc. of MIEL'04, Niš, 2004, Vol. 2, pp. 597-600.

g.94. **Litovski, V.,** Andrejević, M., and Zwolinski, M., "*ANN based modeling, testing, and diagnosis of MEMS*", Proc. of the 7th Seminar on Neural Network Applications in Electronic Engineering, NEUREL 2004, Sept. 2004, Belgrade, pp. 183-188.

g.95. Milenković, S., and **Litovski, V.,** "*Passive image rejection filters optimized for telecommunication applications*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 39-49.

g.96. Litovski, V., Andrejević, M., and Zwolinski, M., "*Acceleration of MEMS fault simulation using ANNs*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 50-54.

g.97. Savić, M., and **Litovski, V.,** "*Bandgap Voltage reference in CMOS*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 55-58.

g.98. Dimitrijević, M., and **Litovski, V.,** "*Implementation of the component characteristic curve tracer using PC-based acquisistion card*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 63-66.

g.99. **Litovski V.,** Andrejevic M., Zwolinski M.,"*Behavioural Modelling, Simulation, Test and Diagnosis of MEMS using ANNs*", 2005 IEEE Int. Symp. on Circuits and Systems, Kobe, Japan, 2005, pp. 5182-5185.

g.100. Dimitrijević,M., and **Litovski, V**.,"*Computer Integrated Analogue Electronics Laboratory for Undergraduate Teaching*", Proc. of the Remote Engineering and Virtual Instrumentation Symposium, REV2005, Brasov, Romania, June 30- July 01, 2005, www.online-lab.net-rev.

g.101. Savić, M., Mrčarica, Ž., and **Litovski, V.,**: "*Computationally Efficient Simulation of Nonlinear Communication Circuits with Switches*", 7th WSEAS Int. Conf. on Mathematical Methods and Computational Techniqeues in Electrical Engineering, WSEAS MMACTEE'05, Sofia, Bulgaria, October 2005, pp. 69-74.

g.102. Sokolović, M., and **Litovski, V.,** "*Using VHDL Simulator to Estimate Logic Path Delays in Combinational and Embedded Sequential Circuits*", IEEE Region 8 EUROCON 2005 Conf., Belgrade, November 21-24, 2005, pp. 1683-1686.

g.103. Dimitrijević,M., and **Litovski, V**., "*Specific analog electronic circuits analysis using PC-based acquisition card*", IEEE Region 8 EUROCON 2005 Conf., Belgrade, November 21-24, 2005, pp. 910-913.

g.104. Andjelković,M., **Litovski, V**., and Zerbe, V., "*New aspects in HDL's performance evaluation*", IEEE Region 8 EUROCON 2005 Conf.,

Belgrade, November 21-24, 2005, pp. 499-502.
g.105. **Litovski, V.,** Milojković, J., and Jovanović, S., "*A concept of education in sustainable electronic design*", Proc. of the Int. Symposium: Waste Management and the Environment III, Malta, June 2006, pp. 415-424. Published by WIT Press, V. Popov, Editor.
g.106. Andjelković,M., **Litovski, V**., and Zerbe, V., "*A Mission Level Design Language Based on Alec++*", Proc. Of the 25th Int. Conf. On Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, 14-17 May, 2006, pp. 659-662.
g.107. **Andrejević, M.,** Litovski, V., and Zwolinski, M., "*Fault Diagnosis in Digital Part of Mixed-Mode Circuits*", Proc. Of the 25th Int. Conf. On Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, 14-17 May, 2006, pp. 437-440.
g.108. Dimitrijević, M., and **Litovski, V.,** «*Power factor and distortion measuring for small loads using USB acquisition module*», Int. Symp. on Remote Engineering and Virtual Instrumentation, REV 2006, Maribor, Slovenia, June 2006. Paper No. SID5.1/2.
g.109. Andrejević, M., and **Litovski, V.,** «*Fault diagnosis in digital part of sigma-delta converter*», Proceedings of the 8th Seminar on Neural network application in electrical engineering, NEUREL ' 2006, pp. 177-180.
g.110. **Litovski, V.,** Andrejević, M., and, Nikolić, M., «*Chaos based analog-to-digital conversion of small signals*», Proceedings of the 8th Seminar on Neural Network Application In Electrical Engineering, NEUREL ' 2006, pp. 173-176.
g.111. Anđelković B., Dimitrijević, M., and **Litovski, V.,** „*Using grid computing in parallel electronic circuit simulation*", Electronics' 2007, 19 – 21 September, Sozopol, Bulgaria, book 4, pp. 109-114.
g.112. Dimitrijević M., and **Litovski, V.,** „*Implementation of compact switching power supply with high power factor*", Electronics' 2007, 19 – 21 September, Sozopol, Bulgaria, pp. 129-132.
g.113. **Litovski, V.,** and Andrejević, M., „*Nonlinear modelling in biomedical applications using ANNs*", Proc. Of the Int. Conf. on Biomedical Electronics and Devices, Biodevices 2008,28. - 31. january 2008., Funchal, Madeira, Portugal, Vol. 1, pp.115-116.
g.114. Andrejević, M., and **Litovski, V.,** „*Hierarchical Approach To Diagnosis Using ANNs* ", Proc. 26th Int. Conf. On Microelectronics (Miel 2008), Niš, Serbia, 11-14 May, 2008, pp. 395-398.
g.115. Sokolović, M., Petković, P., and **Litovski, V.,** "*Design for Testability for SoC Based on IDDQ Scanning*", Proc. 26th Int. Conf. On Microelectronics (Miel 2008), Niš, Serbia , 11-14 May, 2008, pp. 407-410.
g.116. Milojković, J. and **Litovski, V.,** "*Comparison of Some ANN Based*

Forecasting Methods Implemented on Short Time Series", 9th Symposium on Neural Network Applications in Electrical Engineering, NEUREL-2008, Belgrade, 2008, pp. 179-179.

g.117. Milojković, J., and Litovski, V.B., "*Prediction in Electronics based on limited information*", Proceedings of the 8th WSEAS Int. Conf. on Electronics, Hardware, Wireless And Optical Communications, EHAC'09, Cambridge, UK, February 2009, pp. 33-38.

g.118. Petković, P., Trajanov, D., Grnarov, A., and Litovski, V., "*System On Chip Design: New Harmonized Master Studies Curriculum in Macedonia And Serbia*", Ninth National Conf. with Int. Participation, ETAI 2009, Ohrid, Macedonia, September 2009, Proc. on disc, Paper No. IE1-2. ISBN 987-9989-2175-5-5

g.119. Milojković, J. and Litovski, V.B., „*Short-term forecasting of the electricity load at suburban level*", 9th National Conf. with Int. Participation, ETAI 2009, Ohrid, Macedonia, September 2009, Proc. on disc, paper No. A2-1. ISBN 987-9989-2175-5-5

g.120. Litovski, V. B., "*Twenty years of ANN research and application in LEDA*", Small Systems Simulation Symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 33-41.

g.121. Milojković, J., and Litovski, V., "*Multistep forecasting in electronics based on reduced information*", Small Systems Simulation Symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 42-48.

g.122. Anđelković, B., Dimitrijević, M., Andrejević Stošović, M., Litovski, V., "*Parallelizing Electronic Circuit Simulation on Multicore Computer Cluster*", Small Systems Simulation Symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 71-74.

g.123. Dimitrijević, M., and Litovski, V., "*Computer Based Power Factor and Distortion Measuring for Small Loads*", Small Systems Simulation Symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 81-85.

g.124. Milojković, J., Bojanić, S., and Litovski, V., "*On Prediction in Electronics*", Proc. 27th Int. Conf. on Microelectronics (MIEL 2010), Niš, Serbia, 16-19 May, 2010, pp. 275-278.

g.125. Milojković, J., and Litovski, V., **"***New ann models for short term forecasting of electricity loads"*, Proceedings of the 7th EUROSIM Congress on Modelling and Simulation Vol.2: Full Papers (CD), Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Computer Science and Engineering, Prague, Czech Republic ISBN 978-80-01-04589-3, September 2010.

g.126. Milojković, J., and Litovski, V., "*ANN Versus Grey Theory Based Forecasting Methods Implemented on Short Time Series*", 10th Symposium on Neural Network Application in Electrical Engineering, NEUREL-2010,

Faculty of Electrical Engineering, University of Belgrade, Serbia, September 2010, ISBN 978-1-4244-8818-6, pp. 111-116.

g.127. Andrejević Stošović, M., and **Litovski, V.,** " *Hierarchical Approach to Diagnosis of Electronic Circuits using ANNs* ", 10th Symposium on Neural Network Application in Electrical Engineering, NEUREL-2010, Faculty of Electrical Engineering, University of Belgrade, Serbia, September 2010, ISBN 978-1-4244-8818-6, pp. 117-122.

g.128. Milojković, J., **Litovski, V.,** Nieto-Taladriz, O., and Bojanić, S., "*Forecasting Based on Short Time Series Using ANNs and Grey Theory – Some Basic Comparisons*"**,** In Proceedings of the 11th Int. Work-Conf. on Artificial Neural Networks, IWANN 2011, June 2011, Torremolinos-Málaga (Spain). J. Cabestany, I. Rojas, and G. Joya (Eds.): Part I, LNCS 6691, pp. 183–190, 2011, © Springer-Verlag Berlin Heidelberg 2011. ISSN: 0302-9743.

g.129. Milić, M., Andrejević Stošović, M., and **Litovski, V.** ,"*Oscillation Based Analog Testing - A Case Study*", Proc. of the 34th Int. Conv. on Information and communication Technology, Electronics and Microelectronics, MIPRO 2011, Section: Microelectronics, Electronics, and Electronic Technology (MEET), Proc. on a disc, Paper No. 20.

g.130. Milojković, J., and **Litovski, V.,** „*Dynamic One Step Ahead Prediction of Electricity Loads at Suburban Level*", Proc. of the First IEEE Int. Workshop on Smargrid Modeling and Simulation – at IEEE SmartGridComm 2011, SGMS2011, Brussels, October 2011, Proceedings on disc, paper no. 25.

g.131. Lukač, D., Andrejević-Stošović, M., **Litovski, V.**, "*Operating Points and Topographic Dependence of the Thin Layer-Photovoltaic Cells as Relevant Characteristics for Modeling of the PV Cells*", Proceedings of the 4th Small Systems Simulation Symposium, Niš, 2012, ISBN 978-86-6125-059-0, pp. 20-23.

g.132. Andrejević Stošović, M., Lukač, D., **Litovski, V.**, "*Realistic modeling and simulation of the PV system - converter interface*", Proceedings of the 4th Small Systems Simulation Symposium, Niš, 2012, ISBN 978-86-6125-059-0, pp. 28-32.

g.133. Mirković, D., Stevanović, D., **Litovski, V.**, "*Efficient Fault Effect Extraction for an Integrated Power Meter's SigDel ADC*", Proceedings of the 4th Small Systems Simulation Symposium, Niš, 2012, ISBN 978-86-6125-059-0, pp. 125-128.

g.134. Stanojlović, M., and **Litovski, V.**, "*Simulation of defects in the sequential NSDDL Master/Slave D flip flop circuit*", Proceedings of the 4th Small Systems Simulation Symposium, Niš, 2012, ISBN 978-86-6125-059-0, pp. 145-149.

g.135. Dimitrijević, M., and **Litovski, V.**, "*Quantitative Analysis of Reactive Power Definitions for Small Non-linear Loads*", Proceedings of the 4th Small Systems Simulation Symposium, Niš, 2012, ISBN 978-86-6125-059-0, pp. 150-154.

g.136. Lukač, D., Litovski, V., Andrejević-Stošović, M., Vukomirović,S., "*Technology and Light Source as Challenge for proper Modeling of PV Cells*", Proc. of the XI Int. Scientific – Professional Symp. INFOTEH 2012, March 2012, Sarajevo, Bosnia and Herzegovina.

g.137. Milojković, J., Litovski, I., and Litovski, V., "*ANN Application for the Next Day Peak Electricity Load Prediction* ", Proc. of the 11th Symp. on Neural Network Application in Electronic Engineering, NEUREL 2012, Belgrade, Sept. 2012, pp. 237-241.

g.138. Andrejević Stošović, M., Lukač, D., Litovski, I., and Litovski, V., "*Frequency Domain Characterization of a Solar Cell*", Proc. of the 11th Symp. on Neural Network Application in Electronic Engineering, NEUREL 2012, Belgrade, Sept. 2012, pp. 259-264.

g.139. Dimitrijević, M., and Litovski, V., „*Real-time virtual instrument for polyphase nonlinear loads analysis*", Proc. of the IX Int. Symp. On Industrial Electronics, INDEL 2012, Banja Luka, November 2012, pp. 136-141.

g.140. Andrejević Stošović, M., Dimitrijević, M., Litovski, V., and Lukač, D., „*Quantification of Power Quality issues at the PV panel-converter interface*", Proc. of the IX Int. Symp. on Industrial Electronics, INDEL 2012, Banja Vrućica, November 2012, pp. 256-262.

g.141. Milojković, J., and Litovski, V., „*One day ahead peak electricity load prediction*", Proceedings of the IX Int. Symp. On Industrial Electronics, INDEL 2012, Banja Luka, November 2012, pp. 263-267.

g.142 Andrejević Stošović, M., Dimitrijević, M., Litovski, V., "*MPPT Controller Design for a Standalone PV System*", Proc. of the 11th TELSIKS, Niš, October 2013, pp 501-504.

g.143 Milić, M., and Litovski, V., "*Testing Capacitors' Hard Defects in Notch SC Filters Using the Oscillation Method*", Proc. of the 5th Small Systems Simulation Symposium, SSSS'14, Niš, 2014, ISBN 978-86-6125-098-9, pp. 30-36.

g.144 Andrejević Stošović, M., Dimitrijević, M., Litovski, V., "*SPICE Model of a Linear Variable Capacitance*", Proc. of the 5th Small Systems Simulation Symposium, SSSS'14, Niš, 2014, ISBN 978-86-6125-098-9, pp. 43-46.

g.145 Dimitrijević, M., Andrejević Stošović, M., Nieto, O., Bojanić, S., and Litovski, V., "*Computer Workstation Vetting by Supply Current Monitoring*", Proc. of the 5th Small Systems Simulation Symposium, SSSS'14, Niš, 2014, ISBN 978-86-6125-098-9, pp. 113-118.

g.146 Stanojlović, M., Litovski, V., and Petković, P., *"Testing an SCA Hardened Combinational Standard Cell - Preliminary Considerations",* Proc. of the 5th Small Systems Simulation Symposium, SSSS'14, Niš, 2014, ISBN 978-86-6125-098-9, pp. 123-128.

g.147 Milojković, J. and Litovski, V., "*On the method development for electricity load forecasting*", Proc. of 2nd Int. Conf. on Electrical, Electronic and Computing Engineering, Proc. of 1st Int. Conf. on Electrical, Electronic and Computing Engineering IcETRAN 2014, Vrnjačka Banja, Serbia, June 2 – 5, 2014, ISBN 978-86-80509-71-6, pp. ELI1.7.1-5.

g.148 Mirković, D., Petković, P. and Litovski, V., ,"*Experience in Using Open Command Environment for Analysis in Education*", Proc. of 1st Int. Conf on Electrical, Electronic and Computing Engineering IcETRAN 2014, Vrnjačka Banja, Serbia, June 2 – 5, 2014, ISBN 978-86-80509-70-9, pp. ELI 1.8.1-5.

g.149 Litovski I. V, and Litovski, V. B., "*Graphic representation of the synthesis results in a telecommunication-filter design suite*", Proceedings of 2nd Int. Conf. on Electrical, Electronic and Computing Engineering, IcETRAN 2015, Silver Lake, Serbia, June 2015, ISBN 978-86-80509-71-6, pp. ELI1.2.1-6

g.150 Mirković, D., Litovski, I. V., and Litovski, V.B.,"*On the Synthesis and Realization of Selective Linear Phase IIR Filters*", Proc. of 2nd Int. Conf. on Electrical, Electronic and Computing Engineering, IcETRAN 2015, Silver Lake, Serbia, June 8 – 11, 2015, ISBN 978-86-80509-71-6, pp. ELI1.3.1-6.

g.151 Dimitrijević, M.A, Litovski, V. B., "*Characterization of Telecommunication and IT Devices as Nonlinear Loads*", Proc. of 2nd Int. Conf. on Electrical, Electronic and Computing Engineering IcETRAN 2015, Silver Lake, Serbia, June 8 – 11, 2015, ISBN 978-86-80509-71-6 pp. ELI2.1.1-6

g.152 Le Blond, S., Ross, B., and Litovski, V. B.,"*On the implementations of Circuit Models of Arcs*", Proc. of the 6th Small Systems Simulation Symposium, SSSS'16, Niš, 2016, ISBN 978-86-6125-154-2, pp. 16-21.

g.153 Milojković, J., Bojanić, S., Nieto, O., and Litovski, V., "One-Week- and One-Month-Ahead Prediction of Suburban Electricity Load", Proc. of the 6th Small Systems Simulation Symposium, SSSS'16, Niš, 2016, ISBN 978-86-6125-154-2, pp. 104-111.

g.154 Topisirović, D., Andrejević Stošović, M., and Litovski, V., "CMAC and Chebyshev Filters in Frequency Domain", Proc. of the 6th Small Systems Simulation Symposium, SSSS'16, Niš, 2016, ISBN 978-86-6125-154-2, pp. 129-132.

5.h. Papers published at domestic conferences (Papers written in Serbian are marked by an asterix)

h.1.* Lazović, S., **Litovski, V.**, *"Ka problemu aproksimacije konstantnog grupnog kašnjenja"*, XIV Konf. ETAN-a, Sarajevo, Juni, 1970, pp. 25-35.

h.2.* Lazović, S., **Litovski, V.**, *"Jedna nova metoda sinteze prenosne funkcije za kompresiju impulsa"*, XVI Konf. ETAN-a, Velenje, Juni, 1971, pp. 373-381.

h.3.* Lazović, S., **Litovski, V.**, Radmanović,M., *"Automatsko projektovanje niskopropusnih lestvičastih filtara sa zadatim karakteristikama"*, XVIII Konf. ETAN-a, Ulcinj, Juni, 1974 , pp. 290-297.

h.4.* Radmanović, M., **Litovski, V.**, Lazović,S., *"Algoritam za automatsku sintezu prelaznih Thomson-Butterworth-ovih filtara"*, XVIII Konf. ETAN-a, Ulcinj, 1974.

h.5.* **Litovski, V.**, Lazović, S., *"Automatsko projektovanje generalnog fitra"*, XIX Konf. ETAN-a, Ohrid, Juni, 1975, pp. 129-138.

h.6.* **Litovski, V.**, *"Gaussov filtar sa modifikovanom karakterističnom funcijom"*, XX Konf. ETAN-a, Opatija, 1976.

h.7.* **Litovski, V.**, Stojanović, V., Lazović, S., Radmanović, M., *"Realizacija uskopojasnog aktivnog filtra sa specijalnim zahtevima u prelaznoj zoni"*, YUTEL 76, Simp. o telekomunikacijama, Ljubljana, 1976, pp. C/VII-1-C/VII-7.

h.8.* Lazović, S., **Litovski, V.**, *"O jednoj novoj klasi selektivnih filtara sa linearnom faznom karakteristikom"*, XXI Konf. ETAN-a, Banja Luka, Jun, 1977, pp. I.243-I.249.

h.9.* **Litovski, V.**, Milovanović, D., *"Selektivni polinomski filtri sa linearnom faznom karakteristikom"*, Zbornik radova XXI Konf. ETAN-a, Banja Luka, Juni, 1977, pp. I.251-I.257.

h.10.* **Litovski, V.**, Milovanović, D., *"Sinteza neminimalno-faznih filtarskih funkcija s suboptimalnom karakteristikom grupnog kašnjenja"*, Zbornik radova XXII Konf. ETAN-a, Zadar, Juni, 1978, pp. I.289-I.296.

h.11.* **Litovski, V.**, Petković, P., *"Jedan metod simulacije elektronskih kola sa MOS tranzistorima"*, MIEL 79, Simp. o mikroelektronici, Beograd, 1979, pp. 77-83.

h.12.* Milovanović, D., **Litovski, V.**, *"Jedan metod sinteze prenosnih funkcija za prenos podataka"*, Zbornik radova XXIII Konf. ETAN-a, Maribor, Juni, 1979, pp. I.177-I.182.

h.13.* **Litovski, V.**, Lazović, S., *"Jedna nova metoda sinteze filtara sa linearno opadajućim grupnim kašnjenjem"*, XXIII Konf. ETAN-a, Maribor, Juni, 1979, pp. I.169-I.176.

h.14.* Radović, R., **Litovski, V.**, *"Neka iskustva u modeliranju i simulaciji kardiovaskularnog sistema"*, Simp. "Biomedicinska elektronika", Skoplje, april, 1980, pp. 60-85.

h.15.* **Litovski, V.**, Simonović, V., *"Simulacija prelaznih režima u kolima sa MOS tranzistorima"*, MIEL 80, Simp. o mikroelektronici, Niška Banja, april, 1980, pp. 215-221.

h.16.* **Litovski, V.**, Petković, P., *"Razvoj softvera za simulaciju elektronskih kola sa MOS tranzistorima"*, II Znanstveni skup: Numeričke metode u tehnici, Stubičke Toplice, novembar, 1980, pp. 145-155.

h.17.* Milovanović, D., **Litovski, V.**, "*Jedan metod sinteze prenosnih funkcija filtara za prenos govora i impulsa*", Zbornik radova XXV Jug. Konf. ETAN-a, Mostar, juni, 1981, pp. i.165-i.171.

h.18.* **Litovski, V.**, Petković, P., "*Algoritam za kontrolu koraka pri numeričkoj integraciji jednačina elektronskih kola*", III znanstveni skup "Numeričke metode u tehnici", Stubičke toplice, Nov., 1981, pp. 599-607.

h.19.* **Litovski, V.**, Đorđević, S., Stojanović, Z., Petković, P., Pantić, S., "*MOST-program za simulaciju prelaznih režima u kolima sa MOS tranzistorima*", Zbornik radova XXVI Jug. Konf. ETAN-a, Subotica, jun, 1982, pp. i.19-i.26.

h.20.* Damnjanović, M., Milićević, M., **Litovski, V.**, "*Projektovanje integrisanih kola: problem layout-a*", Zbornik radova X Jug. savet. o mikroelektronici, MIEL 82, Banja Luka, april, 1982, pp. 85-116.

h.21.* **Litovski, V.**, Ristić, S., Petković, P., *"Simulacija temperaturske zavisnosti električnih karakteristika kola sa MOS tranzistorima"*, Zbornik radova XXVII Jug. Konf. ETAN-a, Struga, Jun, 1983, pp. II.43-II.48.

h.22.* Damnjanović, M., **Litovski, V.**, *"Povezivanje ćelija u integrisanom kolu"*, Zbornik radova XI Jug. savet. o mikroelektronici MIEL 83, Zagreb, april, 1983, pp. 47-54.

h.23.* Milićević, M., **Litovski, V.**, *"Algoritam za razbijanje ortogonalnih likova na pravougaonike"*, Zbornik radova XII Jug. savet. o mikroelektronici, MIEL 84, Niš, maj, 1984, pp. 203-208.

h.24.* **Litovski, V.**, Petković, P., *"Električna karakterizacija ćelija u gejtovskoj matrici GEM 21"*, Zbornik radova XII Jug. savet. o mikroelektronici, MIEL 84, Niš, 7-9. maj, 1984, pp. 209-214.

h.25.* Milovanović, D., **Litovski, V.**, *"Upotreba modifikovane metode čvorova za simulaciju SC kola u frekventnom i vremenskom domenu"*, Zbornik radova XXVIII Jug. Konf. ETAN-a, Split, Jun, 1984, pp. V.109-V.116.

h.26.* Stojanović, Z., **Litovski, V.**, *"Modeli ćelija u logičkom simulatoru LOST"*, Zbornik radova XIII Jug. savet. o mikroelektronici MIEL 85, Ljubljana, maj, 1985, pp. 115-122.

h.27.* Pantić, S., **Litovski, V.**, *"Programska realizacija električnog modela MOS tranzistora u oblasti zakočenja"*, Zbornik radova XIII Jug. sav. o mikroelektronici, MIEL 85, Ljubljana, 1985, pp. 283-290.

h.28.* Stojanović, Z., **Litovski, V.**, *"Logička simulacija upotrebom programa LOST"*, Zbornik radova XXIX Jug. Konf. ETAN-a, sveska 2, Pronounced the best paper within the section Electronics and awarded the *Branko Raković* award, Niš, Jun, 1985, pp. 21-28.

h.29.* Damnjanović, M., **Litovski, V.**, *"Jedno rešenje problema povezivanja u kanalu gejtovske matrice GEM 21"*, Zbornik radova XXIX Jug. Konf. ETAN-a, Niš, Jun, 1985, pp. VIII.211-VIII.218.

h.30.* **Litovski, V.**, Petković, P., *"Ka simulaciji elektronskih kola visokog stepena integracije"*, Zbornik radova II Tematske Konf. za ETAI, ETAI '85, Ohrid, oktobar, 1985, pp. 1-8.

h.31.* **Litovski, V.**, *"O stanju opreme i programske podrške za projektovanje mikroelektronskih kola u SR Srbiji"*, Zbornik radova savet. "Stanje programske i aparaturne opreme za projektovanje elektronskih kola", Maribor, novembar, 1985, pp. 59-62.

h.32.* Stojanović, Z., **Litovski, V.**, *"Modeliranje kašnjenja logičkih operatora pri različitim nivoima logičke simulacije"*, Zbornik radova XXX Jug. Konf. ETAN-a, Herceg Novi, jun, 1986, pp. II.123-II.130.

h.33.* Petković, P., **Litovski, V.**, *"Makroanaliza vrlo složenih CMOS kola"*, Zbornik radova VIII Medjunarodnog simpozija "Kompjuter na sveučilištu", Cavtat, maj, 1986, pp. 2.15-1 - 2.15-8.

h.34.* Kocić, A., **Litovski, V.**, *"Korišćenje programa za analizu linearnih kola u nastavi"*, Zbornik radova VIII Medjunarodnog simpozija "Kompjutor na sveučilištu", Cavtat, maj, 1986, pp. 1A.02-1 - 1A.02-5.

h.35.* Đorđević, S., **Litovski, V.**, *"Modeliranje i programska realizacija saturacione oblasti bipolarnog tranzistora"*, Zbornik radova XV Jug. savet. o mikroelektronici, MIEL-87, Banja Luka, Maj, 1987, pp. 269-276.

h.36.* **Litovski, V.**, Petković, P., *"Razvoj makromodela CMOS logičkih operatora u vremenskom domenu"*, Zbornik radova XV Jug. Sav. o Mikroelektronici MIEL-87, Banja Luka, Maj, 1987, pp. 55-62.

h.37.* Đorđević, S., **Litovski, V.**, *"Modeliranje i programska realizacija modela bipolarnog tranzistora"*, Zbornik radova XXXI Jug. Konf. ETAN-a, ETAN 87, Bled, Juni, 1987, pp. x.19-x.26.

h.38.* Damnjanović, M., **Litovski, V.**, *"Uticaj redosleda trasiranja veza na konačnu topologiju kanala u gejtovskoj matrici GEM 21"*, Zbornik radova XXXI Jug. konf. ETAN-a, ETAN '87, Bled, Juni, 1987, pp. x.35-x.42.

h.39.* **Litovski, V.**, Milovanović, D., Stojanović, Z., *"Mogućnosti programa ulaznog jezika lostin za logički simulator LOST"*, Zbornik radova XV Jug. sav. o mikroelektronici MIEL 87, Banja Luka, Maj, 1987, pp. 507-512.

h.40.* Milićević, M., **Litovski, V.**, Vacić, Z., Kocić, A., *"Koncepcija razvoja softvera za projektovanje integrisanih kola tipa GEM"*, Zbornik radova Simp.a "Projektiranje i proizvodnja podržani računalom (pppr)", Zagreb, Oktobar, 1987, pp. 435-440.

h.41.* **Litovski, V.**, Đorđević, S., Petković, P., *"Analiza bipolarnih i MOS kola programom MOST"*, Zbornik radova XVI Jug. savet. o mikroelektronici, MIEL 88, Tom I, Zagreb, Maj, 1988, pp. 303-310.

h.42.* Stojanović, Z., **Litovski, V.**, *"Algoritam kontrole toka vremena u logičkom simulatoru LOST"*, Zbornik radova XVI Jug. savet. o mikroelektronici, MIEL 88, Tom I, Zagreb, Maj, 1988, pp. 271-278.

h.43.* Milenković, S., **Litovski, V.**, *"Pregled algoritama za inicijalni razmeštaj ćelija u integrisanom kolu tipa GEM"*, Zbornik radova XXXII Jug. konf. ETAN-a, Sarajevo, 6-10 Jun, 1988, pp. x.123-x.130.

h.44. Radenković, Z., Janković, T., Janićijević, I., **Litovski, V.**, *"SED: An Interactive Symbolic Gate-Array Editor"*, XVII Yugoslav conf. on microelectronics, MIEL 89, Niš, 9-11 Maj, 1989, pp. 577-582.

h.45.* Petković, P., **Litovski, V.**, *"Modeliranje izlazne otpornosti CMOS logičkih operatora"*, III tematski Simp. za ETAI, ETAI '89, Ohrid, Sept., 1989, pp. 29-38.

h.46.* Stojanović, A., **Litovski, V.**, *"Automatizacija projektovanja niskofrekventnih SC-filtara"*, III tematski Simp. za ETAI, ETAI '89, Ohrid, Sept., 1989, pp. 92-100.

h.47.* Milovanović, D., Nikolić, J., Damnjanović, M., **Litovski, V.**, *"Konverzija logičke u topološku šemu integrisanog kola pomoću programa COSILA"*, III tematski simp. za ETAI, ETAI '89, Ohrid, Sept., 1989, pp. 150-159.

h.48.* Janković, T., Radenković, Z., **Litovski, V.**, *"Integrisani softverski paket za projektovanje gejtovske matrice (ISPGM)"*, III tematski simp. za ETAI, ETAI 89, Ohrid, Sept., 1989, pp. 62-71.

h.49.* Milovanović, D., **Litovski, V.**, Petković, P., *"Model Generation Of Faulty Logic Circuits"*, XVII Yugoslav Conf. on microelectronics, MIEL 89, Niš, Maj, 1989, pp. 545-550.

h.50.* Damnjanović, M., **Litovski, V.**, Mrčarica, Ž., *"Programski paket za generisanje veza na integrisanom kolu"*, III tematski Simp. za ETAI, ETAI '89, Ohrid, Septembar, 1989, pp. 72-81.

h.51.* Milovanović, D., Jevtić, M., **Litovski, V.**, *"Modeliranje defekata u sekvencijalnim kolima"*, Zbornik radova XXXIV Jug. Konf. ETAN-a, ETAN '90, Zagreb, Juni, 1990, pp. 137-144.

h.52.* Petković, P., **Litovski, V.**, Glozić, D., *"Novi model izlazne otpornosti CMOS logičkih operatora"*, Zbornik radova XXXIV Jug. Konf. ETAN-a, ETAN '90, Zagreb, 4-8 Juni, 1990, pp. 27-34.

h.53.* Milovanović, D., **Litovski, V.**, *"Modifikovani metod konkurentne simulacije defekata"*, Zbornik radova XXXV Jug. Konf. ETAN-a, Ohrid, Jun, 1991, pp. 195-202.

h.54.* **Litovski, V.**, Rađenović, J., Mrčarica, Ž., Milenković, S., Zografski, Z., *"Modeliranje MOS tranzistora neuronskom mrežom"*, Zbornik radova XXXVI Konf. ETAN-a, Vol. II, Kopaonik, 28.9-1.10, 1992, pp. 19-25.

h.55.* Maksimović, D., Mrčarica, Ž., Glozić, D., Petković, P., **Litovski, V.**, *"Arhitektura programa i strukture podataka u hibridnom simulatoru"*, Zbornik radova XXXVI Konf. ETAN-a, Vol. II, Kopaonik, 28.9-1.10, 1992, pp. 27-34.

h.56.* **Litovski, V.**, Ranđelović, Z., *"Primena greedy strategije pri povezivanju u switchbox-u"*, Zbornik radova XXXVI Konf. ETAN-a, Vol. II, Kopaonik, 28.9-1.10, 1992, pp. 3-9.

h.57.* Milovanović, D., **Litovski, V.**, Jevtić, M., *"Generisanje modela MSD flip-flopa sa defektom"*, Zbornik radova Prve Srpske Konf. o Mikroelektronici i Optoelektronici, MIOPEL '92, Vol. I, Beograd, Oktobar, 1992, pp. 1.3.2.1-1.3.2.8.

h.58.* Ranđelović, Z., **Litovski, V.**, Damnjanović, M., *"Efikasni kanalni algoritam - ECTAN"*, Zbornik radova Prve Srpske Konf. za Mikroelektroniku i Optoelektroniku, MIOPEL '92, Vol. I, Beograd, Okt., 1992, pp. 1.3.1.1-1.3.1.8.

h.59. Mrčarica, Ž., **Litovski, V.**, *"Some Considerations Of Short-Channel MOS Model Selection For A Circuit Simulation Program"*, Zbornik radova Prve Srpske Konf. o Mikroelektronici i Optoelektronici, MIOPEL '92, Vol. I, Beograd, Okt., 1992, pp. 1.3.4.1-1.3.4.6.

h.60.* Bajić, N., Milovanović, D., **Litovski, V.**, Dokić, B., *"Generisanje modela defekata CMOS trostatičkog invertora"*, Zbornik radova Prve Srpske Konf. o Mikroelektronici i Optoelektronici, MIOPEL '92, Vol. I, Beograd, Oktobar, 1992, pp. 1.3.3.1-1.3.3.10.

h.61.* Maksimović, D., Milentijević, I., **Litovski, V.**, *"Projektovanje i logička simulacija cifarsko-serijskog množača"*, Zbornik radova XXXVII Konf. ETAN-a, Beograd, Sept., 1993.

h.62.* Glozić, D., Rađenović, J., **Litovski, V.**, *"Implementacija modela MOS tranzistora modeliranog neuronskom mrežom u hibridnom simulatoru Alecsis"*, Zbornik radova XXXVII Konf. ETAN-a, Beograd, Sept., 1993.

h.63.* Ranđelović, Z., **Litovski, V.**, *"Brzi algoritam za globalno trasiranje"*, Zbornik radova XXXVII Konf. ETAN-a, Vol. II, Beograd, 20-23 Sept., 1993, pp. 195-200.

h.64.* Petković, P., Marković, M., Stevanović, R., Milovanović, D., **Litovski, V.**, *"Primena simboličke analize u projektovanju VF kola"*, TELSIKS '93, Niš, Okt., 1993, pp. VI-15-22.

h.65.* Glozić, D., **Litovski, V.**, *"Primena paketa ASCOTA3 ADIL za projektovanje telekomunikacionih analognih integrisanih kola"*, TELSIKS '93, Niš, Okt., 1993, pp. VI-7-14.

h.66.* Stevanović, R., Petković, P., Milovanović, D., Marković, V., **Litovski, V.**, *"Simbolički pristup analizi vf pojačavača"*, TELSIKS '93, Niš, Okt., 1993, pp. VI-23-30.

h.67.* Maksimović, D., Milentijević, I., **Litovski, V.**, *"Projektovanje i logička simulacija cifarsko-serijskog množača"*, Zbornik radova XXXVII Konf. ETAN-a, Beograd, Sept., 1993, Vol. VIII, pp. 221-226.

h.68.* Zarković, K., **Litovski, V.**, Stojilković, S., *"Ubrzanje učenja veštačkih neuronskih mreža statističkim metodama"*, Zbornik radova XXXVIII Jug. konf. ETRAN-a, Vol. III, Niš, Jun, 1994, pp. 205-206.

h.69.* Maksimović, D., Glozić, D., **Litovski, V.**, *"Trendovi razvoja elektronskih simulatora - Alecsis2.1 hibridni simulator"*, X Scientific Conf. Man and Working Environment: Preventive Engineering and Information Technologies, Niš, Dec., 1994, pp. 25-1-25-8.

h.70.* Milenković, S., Obradović, Z., **Litovski, V.**, *"Dinamičko učenje neuronskih mreža drugog reda zasnovano na simuliranom očvršćavanju"*, 3rd Seminar on Neural Netvork Applications in Electrotechnics NEUREL-95, Belgrade, Yugoslavia, Sep., 1995.

h.71.* Aleksić, D., **Litovski, V.**, Milenković, S., *"Modeliranje i simulacija ethernet bridgea logičkim simulatorom Alecsis 2.1"*, TELSIKS '95, Niš, Okt., 1995, pp. 400-403.

h.72.* Petković, P., Marković, V., **Litovski, V.**, *"Simbolička analiza mikro-talasnih kola u funkciji talasnih parametara"*, TELSIKS '95, Niš, Oct., 1995, pp. 400-403.

h.73.* Ranđelović, Z., **Litovski, V.**, Radović, O., Cvetković, S., *"Simultana konstrukcija Štajnerovog stabla veza pri projektovanju topologije VLSI IC"*, YU INFO '96, Brezovica, April, 1996, pp. 244-247.

h.74.* Milenković,S., Stanković,M., **Litovski,V.**, *"Veštačke neuronske mreže u otkrivanju i dijagnozi otkaza dinamičkih sistema"*, Međunarodna Konf. Tehnički sistemi i sredstva zaštite od požara, eksplozija, havarija i provala, Beograd, Nov., 1996.

h.75.* Milenković, S., Milošević, Z., **Litovski, V.**, Zarković, K., *"Računarske mreže u projektovanju pomoću računara"*, Zbornik radova, IV Telekomunikacioni forum TELFOR '97, Beograd, Sept., 1996, pp. 52-55.

h.76.* **Litovski, V.**, *"Uticaj novih tejnologija u elektronici na razvoj velikih sistema"*, Zbornik radova, XIV naučno stručni Simp. o novim tehnologijama u PTT, Beograd, Dec., 1996, pp. 175-184.

h.77.* Aleksić, D., **Litovski, V.**, Milenković, S., *"Modeliranje i primena modela TCP/IP protokola u Alecsis 2.3 simulatoru"*, Zbornik Radova

YUINFO '97, Brezovica, Apr., 1997, pp 425-428.

h.78. **Litovski, V.**, Milovanović, D., *"Hardware Description Languages For Analog And Mixed-Signal Design"*, Prvi simp. industrijska elektronika INDEL '97, Banja Luka, Sep., 1997, pp. 96-100.

h.79.* Milenković, S., Janković, N., Litovski, I., Živković, V., **Litovski, V.**, Milovanović, D., *"Kolo za power-on-reset u standarnoj CMOS tehnologiji"*, Prvi Simp. industrijska elektronika INDEL '97, Banja Luka, Sept., 1997, pp. 118-123.

h.80.* Janković, S., Maksimović, D., Živković, V., Petković, P., **Litovski, V.**, *"Testabilno digitalno integrisano kolo specifične namene sa ugrađenim analognim multiplekserima"*, Prvi Simp. industrijska elektronika INDEL '97, Banja Luka, Sep., 1997, pp. 124-128.

h.81.* Ranđelović, Z., Zarković, K., **Litovski, V.**, *"Računarsko projektovanje štampanih tkanina"*, Simp. Pravci razvoja tekstilne industrije za treći milenijum, Niš, Okt., 1997, pp. 270-279.

h.82.* Zarković, K., Milenković, S., **Litovski, V.**, *"Primena računarskih mreža pri integraciji CAD sistema u tekstilnoj industriji"*, Simp. Pravci razvoja tekstilne industrije za treći milenijum, Niš, Okt., 1997, pp. 263-269.

h.83.* Milenković, S., **Litovski, V.**, Stanković, M., *"Veštačke neuronske mreže u otkrivanju i dijagnozi otkaza dinamičkih sistema"*, Zbornik radova međunarodne Konf.: Tehnički sistemi i sredstva zaštite od požara, eksplozija, havarija i provala, 1997.

h.84.* Zarković, K., Milenković, S., **Litovski, V.,** "*Primena računarskih mreža pri integraciji informacionih sistema u medicini*", XIII Info-teh '98, Zbornik radova, Vrnjačka Banja, Jun, 1998, pp. 156-160.

h.85.* Đorđević, S., **Litovski, V.**, Petković, P., "*Određivanje granice između frekvencijskih segmenata u okviru segmentne simboličke simulacije*", Drugi Simp. Industrijska Elektronika INDEL '98, Banja Luka, Sep., 1998, pp. 87-92.

h.86.* Petković, P., **Litovski, V.**, Tošić, D., "*Simbolička analiza elektronskih kola, savremeni razvoj i industrijska primena*", Drugi Simp. Industrijska Elektronika, INDEL '98, Banja Luka, Sep., 1998, pp. 11-16.

h.87.* **Litovski, V.,** Damnjanović, M., and Andjelković, B., "*CAD sistemi zasnovani na VHDL okruženju*", VJ INFO 2001, Beograd 03.04.2001, CK VJ, 2001 (publikacija na CD ROMu)

h.88.* Milojković, J., **Litovski, V.,** "*Ekološki aspekt projektovanja u elektronici*", Zbornik radova XLVI konf. ETRAN-a, ETRAN 2002, Jun 2002, Banja Vrućica, pp. I.66-I.79

h.89. **Litovski, V.**, Andrejević, M., "*ANN Application In Modelling of A/D Interfaces for Mixed-Mode Behavioral Simulation*", Proc. of the XLVI Conf. of ETRAN, ETRAN 2002, June 2002, Banja Vrućica, pp. I.51-I.54.

h.90.* Milojković, J., **Litovski, V.**, "*Održivo projektovanje u elektronici*", Proc. of the Int. Conf. on Dependability and Quality Management, DQM-2002, Belgrade, June 2002, pp. 348-354.

h.91. Savić, M., **Litovski, V.**, "*Implementation of a New Object Oriented Frequency Domain Electronic Circuit Simulation System*", Proc. of the IV Symp. Industrial Electronics, INDEL 2002, Banja Luka, Nov. 2002, pp. 166-168.

h.92. Stefanović D., Kayal M., **Litovski V. B.**, "*An Interactive Knowledge Based Analog Design Approach*", Proc. of the IV Symp. Industrial Electronics, INDEL 2002, Banja Luka, November 2002, pp. 173-176.

h.93.* **Litovski, V.**, i Andrejević, M., "*Modelovanje d/a sprege za hibridnu funkcionalnu simulaciju*", Zbornik radove XLV Konf. ETRAN-a, ETRAN 2003, Jun 2003, Herceg Novi, Vol. 1, pp. 76-79.

h.94.* Nikolić, M., i Litovski, V., "*CMOS implementacija hopfildove neuronske mreže*", Zbornik radova XLV Konf. ETRAN-a, ETRAN 2003, Jun 2003, Herceg Novi, Vol. 1, pp. 132-135.

h.95. Savić M., **Litovski, V.**, "*Behavioral object-oriented frequency domain electronic simulation*", VI nacionalna Konf. ETAI,Ohrid, 17.-20. septembar 2003., pp. E1-E4.

h.96. **Litovski, V.**, and Andrejević, M., "*ANN application in electronic circuits diagnosis*", Prod. of the XLVIII ETRAN Conf., Čačak, June 6-10, 2004, Vol. 1, pp. 21-24.

h.97. Zerbe, V., and **Litovski, V.,** "*Design of parallel digital systems and semantic traps*", Prod. of the XLVIII ETRAN Conf., Čačak, June 6-10, 2004, Vol. 1, pp. 91-94.

h.98.* Dimitrijević, M., **Litovski, V.**, Jovanović, S., »*Računarski sistem za izvodjenje laboratorijskih vežbi iz Elektronike*”, V simpozijum industrijska elektronika - INDEL 2004, Banja Luka, ISBN 86-7122-014-1, pp. 156-160.

h.99. Andrejević, M., **Litovski, V.**, Zwolinski, M., »*ANN application in modeling MEMS*”, V simpozijum industrijska elektronika - INDEL 2004, Banja Luka, ISBN 86-7122-014-1, pp. 99-102.

h.100. Savić, M., Ađelković, B., and **Litovski, V.**, »*Parallel mixed-mode simulation – Preliminary study*”, V Simpozijum Industrijska Elektronika - INDEL 2004, Banja Luka, ISBN 86-7122-014-1, pp. 76-79.

h.101.* Sokolović, M., Savić, M., **Litovski, V.**, Jevtić, M., Petković, P., "*Testiranje i dijagnostika A/D konvertora integrisanog merača potrošnje električne energije*", Zbornik radova konferencije INFOTEH-Jahorina, Vol. 4, Ref. E-III-7, March 2005, pp. 349-353.

h.102. Dimitrijević, M. and **Litovski, V.,** "*Implementation of 1MHz Network Analyzer using PC-based Acquisition Card"***,** Zbornik radova XLIX konferencije Etran 2005, Budva, pp.91-94

h.103. **Litovski, V.,** Andelković, B., "*A Comparative Analysis of Design Languages for Hardware-Software Systems"***,** Zbornik radova XLIX konferencije Etran 2005, Budva, pp. 95-98.

h.104. Savić, M., Mrčarica, Ž., and Litovski, V., "*Power electronic circuits simulation using ideal switches* ",13th Int. Symposium on Power Electronics - Ee 2005, XIII Međunarodni simpozijum Energetska elektronika – Ee 2005, Novi Sad, Serbia & Montenegro, November 2nd - 4th, 2005, paper No. T1-1.4, pp. 1-4.

h.105. Milojković, J., and **Litovski, V.,** "*End-of-life management of power electrical components*",13th Int. Symposium on Power Electronics - Ee 2005, XIII Međunarodni simpozijum Energetska elektronika – Ee 2005, Novi Sad, Serbia & Montenegro, November 2nd - 4th, 2005, Paper No. T1-1.7, pp. 1-5.

h.106.* Petković, P., i **Litovski, V.,** "*Koncept integrisanog merača potrošnje električne energije*",13th Int. Symposium On Power Electronics - Ee 2005, XIII Međunarodni simpozijum Energetska elektronika – Ee 2005, Novi Sad, Serbia & Montenegro, November 2nd - 4th, 2005, Paper No. T4-4.6, pp. 1-5.

h.107.* Sokolović, M. i **Litovski, V. B.**:»*Efikasno određivanje statističkog najgoreg slučaja kašnjenja u složenim digitalnim kolima»,* L Konferencija ETRANa, Beograd, Juni 2006. god., pp. EL, 1, 23-26.

h.108. Andrejević, M., Petrović, V., Mirković, D., and **Litovski, V. B.,:** «*Delay defects diagnosis using ANNs*», L Konferencija ETRANa, Beograd, Juni 2006. god., pp. EL, 1, 27-30.

h.109. Savić, M., Mrčarica, Ž., and **Litovski, V.**, «*Implementation nonlinear ideal switch model in SPICE*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 27-31.

h.110. Anđelković, B., and **Litovski, V.** «*Parallel transistor level simulation of electronic circuits on a Beowulf cluster*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 32-35.

h.111. Dimitrijević, M., Anđelković, B., Savić, M., and **Litovski, V.,** «*Gridification and parallelization of electronic circuit simulator*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 95-100.

h.112. Sokolović, M., **Litovski, V.**, and Zwolinski, M., «*Fan-out based delay estimation in digital circuits*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 101-105.

h.113. Andrejević, M., and **Litovski, V.,** «*Fault diagnosis in analog part of*

mixed-mode circuits», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 117-120.

h.114.* Milojković, J. and **Litovski, V.,** *«Program uspostavljanja sistema reciklaže otpadne elektronske opreme od kompjutera*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 121-126.

h.115.* Dimitrijević, M., i Litovski, V., „*Sistem za merenej faktora snage i izobličenja*“, Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 121-126.

h.116. Anđelković, B., **Litovski, V. B.,** and Petković, P., «*Implementation and performance analysis of parallel circuit simulator on BEOWULF cluster*», 51. konferencija za elektroniku, telekomuniklacije, računarstvo, automatiku i nuklearnu tehniku, ETRAN, Herceg Novi, 04-08 Jun, 2007, Rad. EL1.6

h.117.* Milojković, B., i **Litovski, V. B**., «*Novi postupci predviđanja za potrebe održivog razvoja*», 51. konferencija za elektroniku, telekomuniklacije, računarstvo, automatiku i nuklearnu tehniku, ETRAN, Herceg Novi, 04-08 Jun, 2007, Rad. EL1.8

h.118.* Popović, B., i **Litovski, V.,** «*Podizanje kvaliteta nastave iz elektronike putem unapređenja laboratorijskih vežbanja*», 5. Naučno-stručni skup sa međunarodnim učešćem «KVALITET 2007», Neum, BiH, 06.-09 Jun, 2007, Zbornik radova pp. 641-646. Urednik Safet Brdarević. ISSN 1512-9268.

h.119.* **Litovski, V.,** Milojković, J.,**“***Energijska efikasnost u svetlu direktive EC 32 2005*“, XIV Međunarodni simpozijum Energetska Elektronika, Ee 2007, Novi Sad, Srbija, 07.-09. 11.2007. Paper No. T7-2.1, pp. 1-5.

h.120.* Milojković, J., **Litovski, V.,** »*Ponovna upotreba elektronskih proizvoda i projektovanje za ponovnu upotrebu*«, XIV Međunarodni simpozijum Energetska Elektronika, Ee 2007, Novi Sad, Srbija, 07.-09. 11.2007. Paper No. T7-2.4, pp. 1-5.

h.121.* Dimitrijević, M., **Litovski, V.**, „*Izvor napajanja malih gabarita i velikog faktora snage*“, XIV Međunarodni simpozijum Energetska Elektronika, Ee 2007, Novi Sad, Srbija, 07.-09. 11.2007. Paper No. T1-3.2, pp. 1-4.

h.122.* Milojković, J. i **Litovski, V.B.,** „*Postupci predviđanja za ekološke potrebe*“, Ekoist’08, Zbornik radova simpozijuma Ekološka Istina/-Ecological trouth, Juni 2008, Soko Banja, pp. 543-548.

h.123.* Milojković, J. i **Litovski, V.B.**, „*Eko-projektovanje računarske opreme u skladu sa direktivom EC 32 2005*“, ETRAN’08, Zbornik radova LII konferencije ETRANa, Juni 2008, Palić, pp. EL2.1-1-4.

h.124.* Andrejević, Štosović, M., i **Litovski, V.B.,** „*Sinteza hijerarhijskog*

dijagnostičkog sistema za kola sa mešovitim signalima“, ETRAN’08, Zbornik radova LII konferencije ETRANa, Juni 2008, Palić, pp. EL2.2-1-4.

h.125. Litovski, V. and Petković, P.,”*Why The Power Grid Needs Cryptography?*”**,** Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 75-81. **Reprinted in Electronics, Vol. 13, No. 1, June 2009, pp. 30-36.**

h.126.* Sokolović, M., Litovski, V., **”***Statistička analiza kašnjenja asinhronih kola primenom logičkog sumulatora*”, Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 87-92. **Reprinted in Electronics, Vol. 13, No. 1, June 2009, pp. 37-42.**

h.127.* Ćosović, M., i Litovski, V.B., „O jednom konceptu implementacije AES algoritma šifrovanja na FPGA čipu“, Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, Nov., 2008, pp. 82-86.

h.128. Dimitrijević, M., **Litovski, V.**, ”*Virtual Machine Technology in Grid Computing***”,** Zbornik radova VII Simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 240-243.

h.129. Milojković, J., **Litovski, V.**, “*One step ahead prediction in electronics based on limited information*”, ETRAN’09, Zbornik radova LIII konferencije ETRANa, Juni 2009, Vrnjačka Banja, pp. EL 1.7-1-4.

h.130. Milojković, J.B., and Litovski, V.B., “*Short-term forecasting of electricity load using recurrent ANNs*”, 15th Int. Symposium On Power Electronics – Ee2009, Novi Sad, Republic of Serbia, October 28th – 30th, 2009, **ISSN** Paper No. T1-1.7, pp. 1-5. ISBN 86-7892-208-4.

h.131*. Petković, P., i Litovski, V., “Novi Program Diplomskih Akademskih Studija Kao Osnova Za Doktorske Studije Na Elektronskom Fakultetu U Nišu”, XV Conf. Development Trends: “Doctoral Studies In Serbia, Region & EU”, Kopaonik, Serbia, 2-5 March 2009. Joint Tempus Projects Workshop JADES – DEUKS – SoCD, Paper No. W-11, pp. 1-4. (pp. 260-263)

h.132. **Litovski,** V., Nieto-Taldriz, O., Zwolinski, M., Trajanov, D., Bojanić, S., Petković, P., and Grnarov, A., „*TEMPUS JEP-41107 – System on Chip Design, Overview of the realization*“, Proc. Of the XVI Conf.: Development Trends, Kopaonik, Serbia, March 2010, pp. 308-311.

h.133. Petković,P., Stanojlović, M., and **Litovski,**V., "*Design of side-channel-attack resistive criptographic asics*", Zbornik Radova Druge Konferencije o Bezbednosti Informacionih Sistema, Beograd, Forum BISEC 2010,Maj 2010,pp. 22-27.

h.134. **Litovski**,V., Petković, P., and Bojanić, S.,"*Cryptography and the grid*", Zbornik Radova Druge Konferencije o bezbednosti informacionih sistema, Beograd, Forum BISEC 2010, Maj 2010, pp. 93-98.

h.135.* Milojković, J, i **Litovski**, V., „*Novi modeli predviđanja potrošnje lektrične energije zasnovani na VNM*“, Zbornik radova 54. Konferencije za ETRAN, Donji Milanovac, 7-10. juna 2010., Zbornik na disku, ISBN 978-86-80509-65-5 Rad EL1.2, pp.1-4.

h.136.* Andrejević Stošović, M., Dimitrijević, M., **Litovski,**V., “*Implementacija paralelne simulacije elektronskih kola u frekvencijskom domenu* », Zbornik radova 54. Konferencije za ETRAN, Donji Milanovac, 7-10. juna 2010., Zbornik na disku, ISBN 978-86-80509-65-5, Rad EL1.3, pp. 1-4.

h.137.* Dimitrijević, M.A., and **Litovski, V. B.,** “Virtual instrument for three-phase power quality analysis”, Zbornik radova VIII Simpozijuma “Industrijska Elektronika”, INDEL-2010, Novembar 2010, Banja Luka, B&H, pp. 189-194.

h.138.* Milić, M., and **Litovski, V.B.,** “Primena metoda oscilacija za testiranje aktivnog filtra prigušnika opsega frekvencija”, Zbornik radova VIII Simpozijuma “Industrijska Elektronika”, INDEL-2010, Novembar 2010, Banja Luka, B&H, pp. 100-104.

h.139.* Andrejević Stošović, M., Dimitrijević, M., and **Litovski, V.,** “Hyper computing implementation in electronic circuits diagnosis”, Zbornik radova VIII Simpozijuma “Industrijska Elektronika”, INDEL-2010, Novembar 2010, Banja Luka, B&H, pp. 92-95.

h.140.* Milojković**,** J., i **Litovski, V.,** “*Poređenje kratkoročnih predviđanja dobijenih teorijom sivog i neuronskim mrežama*” Zbornik radova 55. Konferencije za ETRAN, Banja Vrućica, 6-9. juna 2011, EL1.3-1-3.

h.141. Andrejević Stošović **,** M., Milić, M., **Litovski, V.,** “*Oscillation based diagnosis implementation in active rc notch filters*”, Zbornik radova 55. Konferencije za ETRAN, Banja Vrućica, Republika Srpska, 6-9. juna 2011, EL1.4-1-4.

h.142.* Milojković, J., Dimitrijević, M., **Litovski, V.,** “*Eko-Projektovanje Elektronske Opreme – Gubici u Standby Režimu*”, XVI Savetovanje Energetska Elektronika – Ee 2011, Novi Sad, Republika Srbija, 26.–28. Oktobar 2011, Rad Br. Ee-1, pp. 1-6.

h.143. Milojković, J., and **Litovski, V.,** “*One step ahead daily electricity peak load prediction based on ANN*”, Zbornik LVI konferencije ETRAN, Zlatibor, ISBN 978-86-80509-67-9, 11.06.-14.06., 2012, EL 3.2.

h.144. Andrejević Stošović, M., Lukač, D., **Litovski, V.,** Milovanović, D., “*Dynamic properties of solar cells*”, Zbornik LVI konferencije ETRAN, Zlatibor, ISBN 978-86-80509-67-9, 11.06.-14.06, 2012, EL4.2

h.145.* Dimitrijević, M., Andrejević Stošović, M. i Litovski, V., „Praćenje, monitoring i kontrola potrošnje električne energije u domaćinstvima“, Zbornik LVII konferencije ETRAN, Zlatibor,2013

h.146. Andrejević Stošović,M., Dimitrijević, *M.,* Lukač, *D.,* and Litovski, *V.,*

"Spice Modeling and Simulation of a Mppt Algorithm", Zbornik LVII konferencije ETRAN, Zlatibor, 2013.

h.147.* Miljana Milić i Vančo Litovski, „*Testiranje parametarskih defekata SC filtarske ćelije prigušnika opsega metodom oscilacija*“ Zbornik LVII konferencije ETRAN, Zlatibor, 2013.

h.148.* Marko Dimitrijević, Miona Andrejević-Stošović, Vančo Litovski, "*Kvantitativna Analiza Reaktivne Snage za Nelinearna Opterećenja*", Naučno-stručni simpozijum Energetska efikasnost, ENEF 2013, Banja Luka, Nov 2013, pp. B1-11-B1-15.

h.149.* Андрејевић Стошовић, М., Димитријевић, Д., и Литовски, В., "*Полиноми са разломљеним степенима, SPICE модел и примена*", Proc. of ETRAN, Vrnjačka Banja, 2014, paper no.

h.150.* Милић, М., и Литовски, В., "*Анализа преносних функција аналогних филтара употребом програма Python*", Proc. of ETRAN, Vrnjačka Banja, 2014, paper no.

h.151.* Stanojlović, M., Petković, P., and Litovski, V., "*Testiranje standardne AND ćelije motporne na bočne napade*", Proc. of ETRAN, Vrnjačka Banja, 2014, paper no.

h.152. Lukač, D., Andrejević Stošović, M., Milovanović, D., and Litovski, V., "*Reference Analysis of the Analogous Models for Photovoltaic Cells by Comparison with the Real Photovoltaic Modules*", X Int. Symp. on Industrial Electronics INDEL 2014, Banja Luka, November 06_08, 2014,pp. 235-240.

h.153. Milić, M., and Litovski, V., "*Python Application for Analyzing Analog Filters' Transfer Function*", X Int. Symp. on Industrial Electronics INDEL 2014, Banja Luka, November 06_08, 2014, pp. 78-82.

h.154 Stanojlović Mirković, M., Litovski, V., Petković, P., and Milovanović, D., "*Faults Simulations in XOR/XNOR Cell Resistant toSide Channel Attacks*", X Int. Symp. on Industrial Electronics INDEL 2014, Banja Luka, November 06_08, 2014, pp. 83-88.

h.155. Milojković, J. and Litovski, V., "*One Month Ahead Prediction of Suburban Average Electricity Load*", Proc. of 2nd Int. Conf. on Electrical, Electronic and Computing Engineering, ETRAN 2015, Silver Lake, Serbia, June 8 – 11, 2015, pp.

h.156* Milojković, J., Litovski, V., Milić, M., „*Predviđanje mesečne potrošnje električne energije na nivou prigradske trafostanice"*, Naučno-stručni simpozijum - Energetska efikasnost - ENEF 2015, Banja Luka, 25.09.-26.09., 2015, str. 70-75, ISBN 978-99955-46-23-6, (M63)

5.i **Papers published at international conferences printed as abstracts**

5.i.1. Petković, P., Marković, V., **Litovski, V.**, *"Analysis Of Complex Microwave Circuits Using SPICE"*, Trans Balck Sea Symposium on Applied Electromagnetism, Metsovo, Greece, 17-19. April, 1996.

5.i.2. Petković, P., Marković, V., **Litovski, V.**, *"Symbolic Analysis Of Complex Microwave Circuits In Terms Of Power Wave Parameters"*, Trans Black Sea Region Symposium on Applied Electromagnetism, Metsovo, Greece, 17-19. April, 1996.

5.i.3. Litovski, V., and Andrejević Stošović, M., „Electronic simulation for the new era“, Advanced Ceramics and Application II Symposium, Serbian Academy of Science, Belgrade, 30 Sept. to 01. Oct. 2013, Book of Abstracts p. 5, Invited presentation.

5.i.4 Milojković, J., Le Blond, S., Mitić, V., Litovski, V., “Implementation of Wide-Bandgap Materials in Power Electronics Components”, Proc. of Abstracts of the Advanced Ceramics and Application Conference, Serbian Academy of Science, Belgrade, Sept. 2016, Invited presentation.

5.j **Papers published at domestic conferences printed as abstracts**

5.j.1.* Vacić, Z., Stanković, T., **Litovski, V.**, *"Jedno rešenje automatskog upravljanja i kontrole sistema sa decentralizovanim pogonom"*, Zbornik radova I naučno-stručnog skupa "Specifični problem projektovanja i izrade finomehaničkih uredjaja", Mašinski fakultet, Niš, septembar, 1981.

5.j.2.* Popović, B., i **Litovski, V.,** “*Koncepti učenja na daljinu primjenjeni na nastavu iz elektronike*”, Program Simpozijuma INFOTEH-Jahorina 2008, Elektrotehnički fakultet Sarajevo, p. 51.

5.j.3. Litovski, V. and Petković, P., „Cryptographic function in the system for remote monitoring and control of expenditure of electricity: why and how”, ICT Forum, RPK Niš, November 2010, na disku.

5.k **Papers published as part of a blog**

5.k.1 Litovski, V., „*Ohm’s Law, Is it I=G·V or V=R·I*”, Yahoo! Voices, http://voices.yahoo.com/ohms-law-12223240.html.

5.k.2 Litovski, V., „*The Ubiquitous Electric Switch, Part 1: Building Digital Circuits*”, Yahoo! Voices, http://voices.yahoo.com/the-ubiquitous-electric-switch-12250199.html?cat=58

5.k.3 Litovski, V., „The *Revolutionary CMOS, Part Two Of: The Ubiquitous Switch*”, Yahoo! Voices, http://voices.yahoo.com/the-revolutionary-cmos-12297901.html?cat=58

6. PHd Dissertation

6.1 **Litovski, V.**, *"Selektivni filtri s monotonom amplitudskom karakteristikom i konstantnim grupnim kašnjenjem u propusnom opsegu"*, Doktorska disertacija, Elektronski fakultet, Niš, 1977.

“Selective filters with monotonic amplitude characteristic and constant group delay in the passband”, University of Niš, 1977.

7. MSc thesis

7.1 **Litovski, V.**, *"Novi metodi sinteze selektivnih filtara s monotonom karakteristikom u propusnom opsegu"*, Magistarska teza, Elektronski fakultet, Niš, 1974.

“New methods of synthesis of selective filters with monotonic amplitude characteristic in the passband”, University of Niš, 1974.

7.2 **Litovski, V.,** "Niskopropusni monotoni selektivni filtri sa svim nulama u beskonačnosti", Magistarski rad, Univerzitet u Nišu, 1973.

"Monotonic Selective Low-pass All-pole Filters", University of Niš, 1973.

8. Reports and technical solutions (Documents written in Serbian are marked by an asterix)

8.1.* **Litovski, V.**, *"Projektovanje C/MOS LSI kola I"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF, 1978, Niš, 1978.

8.2.* **Litovski, V.**, *" Projektovanje C/MOS LSI kola II"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF, 1979, Niš, 1979.

8.3.* **Litovski, V.**, *"Projektovanje C/MOS LSI kola III"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF 1980, Niš, 1980.

8.4.* **Litovski, V.**, Damnjanović,M., *"Projektovanje C/MOS LSI kola IV"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF, 1982), 1982.

8.5.* **Litovski, V.**, Petković, P., *"MOST-program za simulaciju elektronskih kola sa MOS tranzistorima"*, Elektronski fakultet, (Usvojilo Naučno veće Instituta EF, 1984, Preradjeno izdanje štampano 1986), 1984.

8.6.* **Litovski, V.**, Milovanović, D., Damnjanović, M., *"Rezultati istraživanja na projektovanju CMOS IK 1981-1985"*, Grupa autora, Elektronski fakultet, (Umnoženo kao deo izveštaja za istraživački projekt "Mikroelektronske komponente"), Niš, 1985.

8.7.* **Litovski, V.**, Milovanović, D., *"LIFT-program za analizu linearnih elektronskih kola"*, Elektronski fakultet, (Usvojilo Naučno veće Instituta EF, 1984, Preradjeno izdanje štampano 1986), Niš, 1985.

8.8.* **Litovski, V.**, Radenković, T., Radenković, Z., *"SIMGKS - softverski paket koji simulira GKS"*, Grupa autora, deo izveštaja RZNS za projekt "Poluprovodnička mikroelektronika i optoelektronika", Usvojilo Naučno veće Instituta EF, 1986.

8.9.* **Litovski, V.**, Milovanović, D., Stojanović, Z., Milenković, S., *"LIFT II - program za analizu linearnih elektronskih kola sa grafičkim izlazom"*, Grupa autora, Elektronski fakultet, (Umnoženo kao deo izveštaja RZNS za projekt "Poluprovodnička mikroelektronika i optoelektronika"), Niš, 1986.

8.10.* **Litovski, V.**, Petković, P., Milenković, S., Stojanović, Z., *"MOST II - program za analizu linernih kola sa grafičkim izlazom"*, Elektronski fakultet, (umnoženo kao deo izveštaja RZNS za projekt "Poluprovodnička mikroelektronika i optoelektronika"), Niš, 1986.

8.11.* Milovanović, D., Stojanović, Z., Damnjanović, M., **Litovski, V.**, *"Softverski paket za povezivanje logičkog simulatora sa programima za automatsko generisanje topologije"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 17 Decembar, 1987.

8.12.* Milenković, S., Milićević, M., **Litovski, V.**, *"Softverski paket za automatski razmeštaj ćelija na čipu GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 17 Decembar, 1987.

8.13.* Milićević, M., **Litovski, V.**, *"Softverski paket za generisanje PG trake"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 17 Septembar, 1987.

8.14.* Damnjanović, M., **Litovski, V.**, Milovanović, R., *"Softverski paket za automatsko povezivanje na GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 1988.

8.15.* Petković, P., **Litovski, V.**, Stanojević, S., Maksimović, D., Paunović, S., *"Makromodeli složenih logičkih funkcija iz biblioteke ćelija GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1988.

8.16.* Gmitrović, M., **Litovski, V.**, Ranđelović, Z., Radović, O., Kocić, A., *"Softverski paket za modeliranje veza na GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1988.

8.17.* Damnjanović, M., **Litovski, V.**, Milovanović, R., *"Softverski paket za automatsko povezivanje na GEM 500"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1989.

8.18.* Janković, T., Radenković, Z., **Litovski, V.**, *"Integrisani programski paket za projektovanje gejtovskih matrica"*, Usvojila mešovita komisija TOC, VTI i VP8634-1, Decembar, 1989.

8.19.* Petković, P., **Litovski, V.**, Stanojević, S., Maksimović, D., Paunović, S., *"Makromodeli složenih logičkih funkcija iz biblioteke ćelija GEM 500"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1989.

8.20.* Milenković, S., **Litovski, V.**, Đurđanović, O., *"Softverski paket za*

automatski razmeštaj ćelija na čipu GEM 500", Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1989.

8.21.* Gmitrović, M., **Litovski, V.**, Ranđelović, Z., Radović, O., Kocić, A., *"Softverski paket za modeliranje veza na GEM 500"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Novembar, 1989.

8.22.* Glozić, D., Mrčarica, Ž., **Litovski, V.**, Aleksić, D., *"Alecsis2.0 - hibridni simulator"*, 1993, Elektronski fakultet, (interna publikacija).

8.23.* Glozić, D., **Litovski, V.**, *"ASCOTA3 ADIL - sistem za automatsko projektovanje analognih integrisanih kola"*, 1993, Elektronski fakultet, (interna publikacija).

8.24.* Radenković, T., Radenković, Z., **Litovski, V.**, Aleksić, D., *"ISPGM - integrisani softverski paket za projektovanje polja gejtova na X window platformi"*, 1993, Elektronski fakultet. (interna publikacija).

8.25.* **Litovski, V.**, urednik, *"Nove tehnologije u projektovanju integrisanih elektronskih kola"*, Nauka, Beograd, 1994.

8.26. Glozić, D., Maksimović, D., Mrčarica, Ž., Dimić, Ž., **Litovski, V.**, *"Alecsis 2.1 Hybrid Simulator Users Manual"*, LEDA, Faculty of Electronic Engineering, University of Nis, Nis, YU, 1994. (internal publication).

8.27. Glozić, D., Mrčarica, Ž., Maksimović, D., Ilić, T., Dimić, Ž, Aleksić, D., **Litovski, V.**, *"Alecsis, The Simulator"*, LEDA, Faculty of Electronic Engineering, University of Niš, Niš, 1996. (internal publication)

8.28. Mrčarica, Ž., Glozić, D., **Litovski, V.**, Maksimović, D, Ilić, T and Gavrilović, D., "*Alecsis 2.3 the Simualtor for Circuits and Systems, User's Manual*", Elektronski Fakultet (LEDA) Niš, 1998. (internal publication).

8.29. **Litovski, V.B.**, "*Itelligent diagnostic systems, preliminary studies*", Elektronski Fakultet (LEDA) Niš, 2003. (internal publication).

8.30.* **Litovski, V. B.** i ini, "*Program uspostavljanja sistema reciklaže otpadne elektronske opreme od kompjutera*», Agencija za Reciklažu Republike Srbije, Beograd, 2006.

8.31.* Andrejević Stošović, M., **Litovski, V.,** „*Veštačke neuronske mreže u dijagnostici SoC*“, Tehničko rešenje - Nova metoda M85, Elektronski Fakultet u Nišu, br. 07/01-007/11-009 od 30.06.2011.

8.32.* Milić, M., **Litovski, V.,** „*WCA (Worst Case Analzsis) kašnjenja za SoC*“, Tehničko rešenje - Nova metoda M85, Elektronski Fakultet u Nišu, br. 07/01-007/11-010 od 30.06.2011.

8.33.* Milojković, J., **Litovski, V.,** „*Primena VNM u predviđanju*“, Tehničko rešenje - Nova metoda M85, Elektronski Fakultet u Nišu, br. 07/01-007/11-008 od 30.06.2011.

8.34. Dimitrijević, M., and **Litovski, V.,** "*An Advanced Distortion and Power-factor Measuring Device Based on Virtual Instrumentation*", National Instruments Case Study Booklet Eastern Europe, pp. 57-60, 2011.

http://download.ni.com/pub/branches/ee/2011/academic/academic_and_research_days_2010_Booklet/ni_case_study_booklet.pdf

8.35. *Litovski, V. i ini, "*IMPEG2*", Elektronski Fakultet u Nišu, br. 07/01-005/10-058 od 29.04.2010.

8.36. *Litovski, V. i ini, "*IMPEG2-BAQ*", Elektronski Fakultet u Nišu, br. 07/01-005/10-067 od 29.04.2010.

8.37. *Anđelković, B., Dimitrijević, M., Litovski, V., „*Alecsis PG*", Elektronski Fakultet u Nišu, br. 07/01-005/10-068 od 29.04.2010.

8.38.* Milojković, J., Andrejević Stošović, M., and Litovski, V., "*A procedure for prediction of the daily peak consumption of electrical energy (Поступак Предвиђања Вршне Вредности Дневне Потрошње Електричне Енергије)*", Elektronski Fakultet u Nišu, No. 07/05-016/14-001 at 09.01.2014.

8.39. * Stanojlović, M, Litovski, V., and Petković, P., "A method for realistic creation of fault dictionaries in CMOS circuits (*Метод реалистичног креирања речника дефеката у CMOS колима)*", Elektronski Fakultet u Nišu, No. 07/05-006/14-005 of 09.01.2014.

8.40.* Andrejević Stošović, M., Milić, M., and Litovski, V., "Analog filter diagnosis using the oscillation method (*Дијагностика аналогних филтара коришћењем методе осцилација)*", Elektronski Fakultet u Nišu, No. 07/05-006/14-009 of 09.01.2014.

8.41. * Milić, M., Andrejević Stošović, M., and Litovski, V "(Application of the oscillation method for testing the active notch filter (*Примена метода осцилација за тестирање активног филтра, непропусника опсега фреквенција)*" Elektronski Fakultet u Nišu, No. 07/05-006/14-003 of 09.01.2014.

8.42* Andrejević Stošović, M., Dimitrijević, M., Milojković, J., and Litovski, V, "*Design of circuit for monitoring of an autonomous photovoltaic system*" ("Пројектовање кола за праћење максималне снаге самосталног фотонапонског система"), тех. решење, ННВ ЕФ бр. 07/10-006/14-001 од 26.12.2014. год.

9. Teaching publications

9.1.* **Litovski, V.**, *"Zbirka zadataka iz projektovanja elektronskih kola"*, Naučni podmladak, Niš, 1978.

9.2.* **Litovski, V.**, Lazović, S., *"Uvod u elektroniku I deo"*, Institut za naučno-tehničku dokumentaciju Zaštite na radu, Niš, 1981.

9.3.* **Litovski, V.**, *"Projektovanje elektronskih kola pomoću računara"*, Univerzitet u Nišu, 1981.

9.4.* **Litovski, V.**, Petković, P., *"Zbirka zadataka iz projektovanja*

elektronskih kola", drugo dopunjeno izdanje, Univerzitet u Nišu, 1981.
9.5.* **Litovski, V.**, Lazović, S., *"Uvod u elektroniku, II deo"*, Univerzitet u Nišu, 1983.
9.6.* **Litovski, V.**, Radmanović, M., Petković, P., Pavlović, V., *"Praktikum labaratorijskih vežbanja iz fizičkih osnova elektronike"*, Univerzitet u Nišu, 1983.
9.7.* **Litovski, V.**, Lazović, S., *"Uvod u elektroniku, II deo"*, ponovljeno nepromenjeno izdanje, Univerzitet u Nišu, 1988.
9.8.* **Litovski, V.**, Lazović, S., *"Elektronika I, prvi deo"*, Naučna knjiga, Beograd, 1989.
9.9.* **Litovski, V.**, *"CADEC1: Analiza i optimizacija elektronskih kola"*, Naučna knjiga, Beograd, 1989.
9.10.* Lazović, S., **Litovski, V.**, *"Elektronika I, drugi deo"*, Naučna Knjiga, Beograd, 1990.
9.11.* **Litovski, V.**, Lazović, S., *"Elektronika I, prvi deo"*, Nauka, Beograd, 1991.
9.12.* **Litovski, V.**, Petković, P., Milenković, S., Milovanović, D., Glozić, D., Mrčarica, Ž., Maksimović, D., Ranđelović, Z., *"Praktikum laboratorijskih vežbanja iz Elektronike I"*, Nauka, Beograd, 1992, do sada je izdanje ponovljeno četiri puta .
9.13.* **Litovski, V.**, Petković, P., Milovanović, D., Milenković, S., Damnjanović, M., *"CADEC2: Simulacija i projektovanje topologije integrisanih kola"*, Nauka, Beograd, 1992.
9.14. **Litovski, V.**, Zwolinski, M., *"VLSI Circuit Simulation And Optimization"*, Chapman and Hall, London, 1997.
9.15.* **Litovski, V.**, Lazović, S., *"Osonovi elektronike"*, Čuperak Plavi, Niš, 1996. Ponovo štampano 2003 god.
9.16.* Maksimović, D., Janković, S., Milenković, S., Ranđelović, Z., Petković, P., Damnjanović,M., **Litovski,V.**, *"Projektovanje elektronskih kola"*, Laboratorijski praktikum, Elektronski fakultet Niš, 1996.
9.17.* **Litovski, V.,** Milovanović, D., Petković, P., Milenković, S., Randjelović, Z., Panić, V., i Ilić, T., "*Zbornik rešenih zadataka iz osnova elektronike*", Niš, Čuperak Plavi, 1997.
9.18.* **Litovski, V.B.**, "*Projektovanje elektronskih kola, Simulacija, Optimizacija, Testiranje i Fizičko projektovanje*", Nova Jugoslavija, Vranje, 2000.
9.19.* Damnjanović, M, urednik. **Litovski, V.**, Damnjanović, M., Jevtić, M., Milovanović, D., Petković, P., Mrčarica, Ž., Djordjević, G., Maksimović, D., Janković, S., Panić, V., Živković, V., i Leković, B., "*Praktikuma laboratorijskih vezbanja ia projektovanja i testiranja elektronskih kola i sistema*", Elektronski fakultet, Niš, 2000.

9.20. **Litovski, V.,** editor, “Proceedings of the Colloquium on Higher education of Electronics in Serbia”, LEDA 2004, ISBN 86-80135-88-7.
9.21.* **Litovski, V.**, *"Osonovi elektronike, Teorija rešeni zadaci i ispitna pitanja"*, Akademska Misao, Beograd, 2006. god. (http://litovski.com/).

http://www.amazon.com/gp/pdp/profile/A3HZNQ2LB7R9OH

 VLSI Circuit Simulation and Optimization by V. Litovski	★★★★★ **A really good book to read and have !!!**, June 30, 2005 An excellent book on topics in EDA field. The book is so carefully written that it can inspire its readers to come up with some new circuit simulators. Both analog and digital circuit simulation are covered, and the chapters on matrix treatment, software implementation are specially recommended. What is a little confusing about the book is that the title of "VLSI circuit" somewhat seems to be talking about VLSI digital circuit simulation stuff. However, the book is indeed for study in analog circuit simulation algorithms mostly. The last several chapters do cover some topics in digital circuit simulation. Overall, it is an amazing book to... Read more

9.22.* **Litovski, V.**, “Osnovi testiranja elektronskih kola”, Elektronski fakultet, Niš, ISBN 978-86-85195-71-6, 2009.
9.23.* **Litovski, V.**, „Modelovanje komponenata elektronskih kola i sistema“, Elektronski fakultet, Niš, ISBN 978-86-85195-75-4, 2009.
9.24.* Milić, M., Andrejević Stošović, M., **Litovski, V.,** „Praktikum laboratorijskih vežbi iz testiranja i dijagnostike elektronskih kola“, Elektronski Fakultet, Niš, 2010, ISBN 978-86-6125-007-1.
9.25.* **Litovski, V.,** „Zbirka zadataka iz testiranja elektronskih kola“, Elektronski fakultet u Nišu, Niš, 2010, ISBN 978-86-6125-008-8.

10. Reviews of books

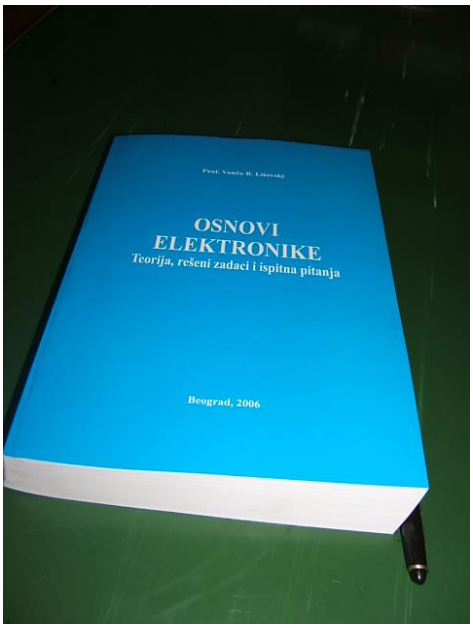
1. **Litovski, V.**, *"The VHDL Handbook"*, Coehlo, D.R., *J. of Semicustom IC's, Vol. 8, No. 3, Book Rewiew, March, 1991, pp. 53.*
2. **Litovski, V.**, *"VHDL: Hardware Description And Design"*, Lipsett, R., Schaefer, C., and Ussery, C., *J. of Semicustom IC's, Vol. 8, No. 3, Book Review, March, 1991, pp. 53.*
3. **Litovski, V.**, Pantić, S., *"The Verilog Hardware Description Language"*, Donald E. Thomas and Philip Moorby, *Microelectronics J., Vol.23, No.4, Book review, July, 1992, pp. 316-317.*
4. **Litovski, V.**, Pantić, S., *"Hardware Design And Simulation In VAL/VHDL"*, L.M. Augustin, D.C. Luckham, B.A. Gennart, Y. Huk and A.G. Stanculescu, *Microelectronics J., Vol.23, No.4, Book review, July, 1992, pp. 316.*
5. Litovski, V. B., Damnjanović, M., "Discrete events simulation in C", Kevin Watkins, McGraw-Hill, Maidenhead, 1993, *Microelectronics Journal, Vol. 25, No.5, Book review, 1994, pp. 402-403.*

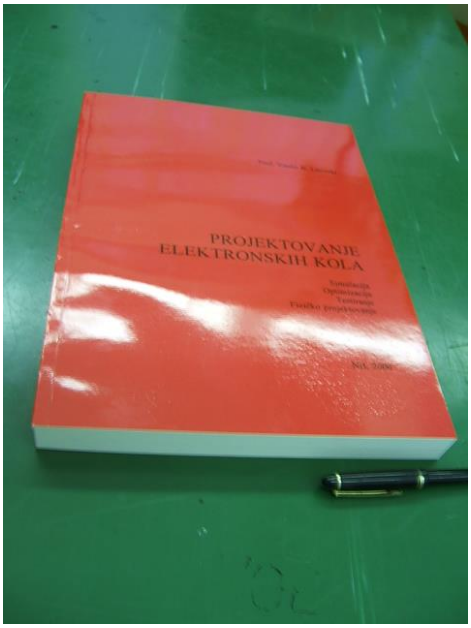
11. Prologue to a book and editing journals and symposia

1. Nančeva Filipova, K., et all., "Ispolzovanie na (v) HDL za sintez na elektronenharduer" KING-2001, ISBN 954-9518-21-3.
2. „Electronics", ISSN 1450-5643, Vol. 8, No. 2, December 2004.
3. Proceedings of the XLVI Conf. of ETRAN, Belgrade 2002, ISBN 86-80509-41-8.

Originals of the books

4. 50 Years of Cooperation Between Faculty of Electronic Engineering in Niš and Faculty of Electrical Engineering in Banja Luka, Plenary Paper, IX Symposium Industrial Electronics INDEL 2012, Banja Luka, November 01_03, 2012.
5. Litovski, V., "Electronics", in "ЕТ(Р)АН, Првих шездесет конференција, Допринос развоју електротехничке струке", edited by B. Milovanović, B., and Jakšić, Z., Belgrade 2016, Published by ETRAN, pp. 1-10 (in Serbian).





12. List of doctoral students (The text are all in Serbian)

R. B.	Title	Name of the candidate	Subm-itted	Defe-nded
1*	Macromodeling and macroanalysis of CMOS LSI electronic circuits	Predrag Petković		1990
2*	Modeliranje i simulacija defekata u CMOS integrisanim kolima modifikovanom konkurentnom metodom	Dragiša Milovanović		1991
3*	Novi algoritmi za projektovanje veza u integrisanim kolima tipa GEM	Milunka Damnjanović		1991
4	ALECSIS 2.1 – Objektno orijentisani hibridni simulator	Dejan Glozić		1994
5	Dinamičko učenje neuronskih mreža drugog reda zasnovano na simuliranom očvršćavanju	Srđan Milenković		1996
6	Logička simulacija - procena graničnih svojstava projekto-vanog digitalnog kola	Dejan Maksimović		2000

7	Novi postupci projektovanja i primene mikrokontrolera u automobilskim aplikacijama	Saša Janković		2005
8	Primena veštačkih neuronskih mreža u dijagnostici elektronskih kola	Miona Andrejević Stošović		2006
9	Primena nelinearnog modela idealnog prekidača u simulaciji elektronskih kola	Milan Savić		2007
10	Određivanje statistički najnepo-voljnijeg slučaja kašnjenja u digitalnim kolima upotrebom logičkog simulatora	Miljana Sokolović	2007	2009
11	Paralelizacija i gridifikacija simulatora elektronskih kola i sistema sa mešovitim signalima	Bojan Anđelković	2007	x
12	Predviđanje u elektronici pomoću veštačkih neuronskih mreža zasnovano na ograničenoj informaciji	Jelena Milojković	2009	2010
13	Elektronski sistem za analizu polifaznih opterećenja baziran na FPGA	Marko Dimitrijević	2011	2012